Power Electronic Devices

1 Power Electronics  Kaushik Rajashekara, Sohail Anwar, Vrej Barkhordarian, Alex Q. Huang
Overview • Diodes • Schottky Diodes • Thyristors • Power Bipolar Junction
Transistors • MOSFETs • General Power Semiconductor Switch Requirements • Gate
Turn-Off Thyristors • Insulated Gate Bipolar Transistors • Gate-Commutated Thyristors
and Other Hard-Driven GTOs • Comparison Testing of Switches
1.1 Overview
Thyristor and Triac • Gate Turn-Off Thyristor • Reverse-Concepting Thyristor (RCT) and Asymmetrical Silicon-Controlled Rectifier (ASCR) • Power Transistor • Power MOSFET • Insulated-Gate Bipolar Transistor (IGBT) • MOS-Controlled Thyristor (MCT)

1.2 Diodes
Characteristics • Principal Ratings for Diodes • Rectifier Circuits • Testing a Power Diode • Protection of Power Diodes

1.3 Schottky Diodes
Characteristics • Data Specifications • Testing of Schottky Diodes

1.4 Thyristors
The Basics of Silicon-Controlled Rectifiers (SCR) • Characteristics • SCR Turn-Off Circuits • SCR Ratings • The DIAC • The Triac • The Silicon-Controlled Switch • The Gate Turn-Off Thyristor • Data Sheet for a Typical Thyristor

1.5 Power Bipolar Junction Transistors
The Volt-Ampere Characteristics of a BJT • BJT Biasing • BJT Power Losses • BJT Testing • BJT Protection

1.6 MOSFETs
Static Characteristics • Dynamic Characteristics • Applications

1.7 General Power Semiconductor Switch Requirements

1.8 Gate Turn-Off Thyristors
GTO Forward Conduction • GTO Turn-Off and Forward Blocking • Practical GTO Turn-Off Operation • Dynamic Avalanche • Non-Uniform Turn-Off Process among GTO Cells • Summary

1.9 Insulated Gate Bipolar Transistors
IGBT Structure and Operation

1.10 Gate-Commutated Thyristors and Other Hard-Driven GTOs
Unity Gain Turn-Off Operation • Hard-Driven GTOs

1.11 Comparison Testing of Switches
Pulse Tester Used for Characterization • Devices Used for Comparison • Unity Gain Verification • Gate Drive Circuits • Forward Conduction Loss Characterization • Switching Tests • Discussion • Comparison Conclusions
1.1 Overview

Kaushik Rajashekara

The modern age of power electronics began with the introduction of thyristors in the late 1950s. Now there are several types of power devices available for high-power and high-frequency applications. The most notable power devices are gate turn-off thyristors, power Darlington transistors, power MOSFETs, and insulated-gate bipolar transistors (IGBTs). Power semiconductor devices are the most important functional elements in all power conversion applications. The power devices are mainly used as switches to convert power from one form to another. They are used in motor control systems, uninterruptible power supplies, high-voltage DC transmission, power supplies, induction heating, and in many other power conversion applications. A review of the basic characteristics of these power devices is presented in this section.

Thyristor and Triac

The thyristor, also called a silicon-controlled rectifier (SCR), is basically a four-layer three-junction \textit{pnpn} device. It has three terminals: anode, cathode, and gate. The device is turned on by applying a short pulse across the gate and cathode. Once the device turns on, the gate loses its control to turn off the device. The turn-off is achieved by applying a reverse voltage across the anode and cathode. The thyristor symbol and its volt–ampere characteristics are shown in Fig. 1.1. There are basically two classifications of thyristors: converter grade and inverter grade. The difference between a converter-grade and an inverter-grade thyristor is the low turn-off time (on the order of a few microseconds) for the latter. The converter-grade thyristors are slow type and are used in natural commutation (or phase-controlled) applications.

FIGURE 1.1  (a) Thyristor symbol and (b) volt–ampere characteristics. (From Bose, B.K., \textit{Modern Power Electronics: Evaluation, Technology, and Applications}, p. 5. © 1992 IEEE. With permission.)
Inverter-grade thyristors are used in forced commutation applications such as DC-DC choppers and DC-AC inverters. The inverter-grade thyristors are turned off by forcing the current to zero using an external commutation circuit. This requires additional commutating components, thus resulting in additional losses in the inverter.

Thyristors are highly rugged devices in terms of transient currents, $di/dt$, and $dv/dt$ capability. The forward voltage drop in thyristors is about 1.5 to 2 V, and even at higher currents of the order of 1000 A, it seldom exceeds 3 V. While the forward voltage determines the on-state power loss of the device at any given current, the switching power loss becomes a dominating factor affecting the device junction temperature at high operating frequencies. Because of this, the maximum switching frequencies possible using thyristors are limited in comparison with other power devices considered in this section.

Thyristors have $I^2t$ withstand capability and can be protected by fuses. The nonrepetitive surge current capability for thyristors is about 10 times their rated root mean square (rms) current. They must be protected by snubber networks for $dv/dt$ and $di/dt$ effects. If the specified $dv/dt$ is exceeded, thyristors may start conducting without applying a gate pulse. In DC-to-AC conversion applications, it is necessary to use an antiparallel diode of similar rating across each main thyristor. Thyristors are available up to 6000 V, 3500 A.

A triac is functionally a pair of converter-grade thyristors connected in antiparallel. The triac symbol and volt–ampere characteristics are shown in Fig. 1.2. Because of the integration, the triac has poor reapplied $dv/dt$, poor gate current sensitivity at turn-on, and longer turn-off time. Triacs are mainly used in phase control applications such as in AC regulators for lighting and fan control and in solid-state AC relays.

**Gate Turn-Off Thyristor**

The GTO is a power switching device that can be turned on by a short pulse of gate current and turned off by a reverse gate pulse. This reverse gate current amplitude is dependent on the anode current to be turned off. Hence there is no need for an external commutation circuit to turn it off. Because turn-off is provided by bypassing carriers directly to the gate circuit, its turn-off time is short, thus giving it more capability for high-frequency operation than thyristors. The GTO symbol and turn-off characteristics are shown in Fig. 1.3.

GTOs have the $I^2t$ withstand capability and hence can be protected by semiconductor fuses. For reliable operation of GTOs, the critical aspects are proper design of the gate turn-off circuit and the snubber circuit. A GTO has a poor turn-off current gain of the order of 4 to 5. For example, a 2000-A peak current GTO may require as high as 500 A of reverse gate current. Also, a GTO has the tendency to latch at temperatures above 125°C. GTOs are available up to about 4500 V, 2500 A.
Reverse-Conducting Thyristor (RCT) and Asymmetrical Silicon-Controlled Rectifier (ASCR)

Normally in inverter applications, a diode in antiparallel is connected to the thyristor for commutation/freewheeling purposes. In RCTs, the diode is integrated with a fast switching thyristor in a single silicon chip. Thus, the number of power devices could be reduced. This integration brings forth a substantial improvement of the static and dynamic characteristics as well as its overall circuit performance.

The RCTs are designed mainly for specific applications such as traction drives. The antiparallel diode limits the reverse voltage across the thyristor to 1 to 2 V. Also, because of the reverse recovery behavior of the diodes, the thyristor may see very high reapplied \( \frac{dv}{dt} \) when the diode recovers from its reverse voltage. This necessitates use of large RC snubber networks to suppress voltage transients. As the range of application of thyristors and diodes extends into higher frequencies, their reverse recovery charge becomes increasingly important. High reverse recovery charge results in high power dissipation during switching.

The ASCR has similar forward blocking capability to an inverter-grade thyristor, but it has a limited reverse blocking (about 20 to 30 V) capability. It has an on-state voltage drop of about 25% less than an inverter-grade thyristor of a similar rating. The ASCR features a fast turn-off time; thus it can work at a higher frequency than an SCR. Since the turn-off time is down by a factor of nearly 2, the size of the commutating components can be halved. Because of this, the switching losses will also be low.

Gate-assisted turn-off techniques are used to even further reduce the turn-off time of an ASCR. The application of a negative voltage to the gate during turn-off helps to evacuate stored charge in the device and aids the recovery mechanisms. This will, in effect, reduce the turn-off time by a factor of up to 2 over the conventional device.

**FIGURE 1.3** (a) GTO symbol and (b) turn-off characteristics. (From Bose, B.K., Modern Power Electronics: Evaluation, Technology, and Applications, p. 5. © 1992 IEEE. With permission.)
Power Transistor

Power transistors are used in applications ranging from a few to several hundred kilowatts and switching frequencies up to about 10 kHz. Power transistors used in power conversion applications are generally npn type. The power transistor is turned on by supplying sufficient base current, and this base drive has to be maintained throughout its conduction period. It is turned off by removing the base drive and making the base voltage slightly negative (within $-V_{BE(max)}$). The saturation voltage of the device is normally 0.5 to 2.5 V and increases as the current increases. Hence, the on-state losses increase more than proportionately with current. The transistor off-state losses are much lower than the on-state losses because the leakage current of the device is of the order of a few milliamperes. Because of relatively larger switching times, the switching loss significantly increases with switching frequency. Power transistors can block only forward voltages. The reverse peak voltage rating of these devices is as low as 5 to 10 V.

Power transistors do not have $I^2t$ withstand capability. In other words, they can absorb only very little energy before breakdown. Therefore, they cannot be protected by semiconductor fuses, and thus an electronic protection method has to be used.

To eliminate high base current requirements, Darlington configurations are commonly used. They are available in monolithic or in isolated packages. The basic Darlington configuration is shown schematically in Fig. 1.4. The Darlington configuration presents a specific advantage in that it can considerably increase the current switched by the transistor for a given base drive. The $V_{CE(sat)}$ for the Darlington is generally more than that of a single transistor of similar rating with corresponding increase in on-state power loss. During switching, the reverse-biased collector junction may show hot-spot breakdown effects that are specified by reverse-bias safe operating area (RBSOA) and forward-bias safe operating area (FBSOA). Modern devices with highly interdigitated emitter base geometry force more uniform current distribution and therefore considerably improve secondary breakdown effects. Normally, a well-designed switching aid network constrains the device operation well within the SOAs.

Power MOSFET

Power MOSFETs are marketed by different manufacturers with differences in internal geometry and with different names such as MegaMOS, HEXFET, SIPMOS, and TMOS. They have unique features that make them potentially attractive for switching applications. They are essentially voltage-driven rather than current-driven devices, unlike bipolar transistors.

The gate of a MOSFET is isolated electrically from the source by a layer of silicon oxide. The gate draws only a minute leakage current on the order of nanoamperes. Hence, the gate drive circuit is simple and power loss in the gate control circuit is practically negligible. Although in steady state the gate draws virtually no current, this is not so under transient conditions. The gate-to-source and gate-to-drain
capacitances have to be charged and discharged appropriately to obtain the desired switching speed, and
the drive circuit must have a sufficiently low output impedance to supply the required charging and
discharging currents. The circuit symbol of a power MOSFET is shown in Fig. 1.5.

Power MOSFETs are majority carrier devices, and there is no minority carrier storage time. Hence,
they have exceptionally fast rise and fall times. They are essentially resistive devices when turned on,
while bipolar transistors present a more or less constant $V_{CE(sat)}$ over the normal operating range. Power
dissipation in MOSFETs is $I_d^2 R_{DS(on)}$, and in bipolars it is $I_c V_{CE(sat)}$. At low currents, therefore, a power
MOSFET may have a lower conduction loss than a comparable bipolar device, but at higher currents,
the conduction loss will exceed that of bipolars. Also, the $R_{DS(on)}$ increases with temperature.

An important feature of a power MOSFET is the absence of a secondary breakdown effect, which is
present in a bipolar transistor, and as a result, it has an extremely rugged switching performance. In
MOSFETs, $R_{DS(on)}$ increases with temperature, and thus the current is automatically diverted away from
the hot spot. The drain body junction appears as an antiparallel diode between source and drain. Thus,
power MOSFETs will not support voltage in the reverse direction. Although this inverse diode is relatively
fast, it is slow by comparison with the MOSFET. Recent devices have the diode recovery time as low as
100 ns. Since MOSFETs cannot be protected by fuses, an electronic protection technique has to be used.

With the advancement in MOS technology, ruggedized MOSFETs are replacing the conventional
MOSFETs. The need to ruggedize power MOSFETs is related to device reliability. If a MOSFET is operating
within its specification range at all times, its chances for failing catastrophically are minimal. However,
if its absolute maximum rating is exceeded, failure probability increases dramatically. Under actual
operating conditions, a MOSFET may be subjected to transients—either externally from the power bus
supplying the circuit or from the circuit itself due, for example, to inductive kicks going beyond the
absolute maximum ratings. Such conditions are likely in almost every application, and in most cases are
beyond a designer’s control. Rugged devices are made to be more tolerant for overvoltage transients.
Ruggedness is the ability of a MOSFET to operate in an environment of dynamic electrical stresses,
without activating any of the parasitic bipolar junction transistors. The rugged device can withstand
higher levels of diode recovery $dv/dt$ and static $dv/dt$.

**Insulated-Gate Bipolar Transistor (IGBT)**

The IGBT has the high input impedance and high-speed characteristics of a MOSFET with the conductivity
characteristic (low saturation voltage) of a bipolar transistor. The IGBT is turned on by applying a positive
voltage between the gate and emitter and, as in the MOSFET, it is turned off by making the gate signal
zero or slightly negative. The IGBT has a much lower voltage drop than a MOSFET of similar ratings.
The structure of an IGBT is more like a thyristor and MOSFET. For a given IGBT, there is a critical value of collector current that will cause a large enough voltage drop to activate the thyristor. Hence, the device manufacturer specifies the peak allowable collector current that can flow without latch-up occurring. There is also a corresponding gate source voltage that permits this current to flow that should not be exceeded.

Like the power MOSFET, the IGBT does not exhibit the secondary breakdown phenomenon common to bipolar transistors. However, care should be taken not to exceed the maximum power dissipation and specified maximum junction temperature of the device under all conditions for guaranteed reliable operation. The on-state voltage of the IGBT is heavily dependent on the gate voltage. To obtain a low on-state voltage, a sufficiently high gate voltage must be applied.

In general, IGBTs can be classified as punch-through (PT) and nonpunch-through (NPT) structures, as shown in Fig. 1.6. In the PT IGBT, an $N^+$ buffer layer is normally introduced between the $P^+$ substrate and the $N^-$ epitaxial layer, so that the whole $N^-$ drift region is depleted when the device is blocking the off-state voltage, and the electrical field shape inside the $N^-$ drift region is close to a rectangular shape. Because a shorter $N^-$ region can be used in the punch-through IGBT, a better trade-off between the forward voltage drop and turn-off time can be achieved. PT IGBTs are available up to about 1200 V.

High-voltage IGBTs are realized through a nonpunch-through process. The devices are built on an $N^-$ wafer substrate which serves as the $N^-$ base drift region. Experimental NPT IGBTs of up to about 4 kV have been reported in the literature. NPT IGBTs are more robust than PT IGBTs, particularly under short circuit conditions. But NPT IGBTs have a higher forward voltage drop than the PT IGBTs.

The PT IGBTs cannot be as easily paralleled as MOSFETs. The factors that inhibit current sharing of parallel-connected IGBTs are (1) on-state current unbalance, caused by $V_{CE(sat)}$ distribution and main circuit wiring resistance distribution, and (2) current unbalance at turn-on and turn-off, caused by the switching time difference of the parallel connected devices and circuit wiring inductance distribution. The NPT IGBTs can be paralleled because of their positive temperature coefficient property.
The MCT is a new type of power semiconductor device that combines the capabilities of thyristor voltage and current with MOS gated turn-on and turn-off. It is a high-power, high-frequency, low-conduction drop and a rugged device, which is more likely to be used in the future for medium and high power applications. A cross-sectional structure of a $p$-type MCT with its circuit schematic is shown in Fig. 1.7. The MCT has a thyristor type structure with three junctions and $pnps$ layers between the anode and cathode. In a practical MCT, about 100,000 cells similar to the one shown are paralleled to achieve the desired current rating. MCT is turned on by a negative voltage pulse at the gate with respect to the anode, and is turned off by a positive voltage pulse.

The MCT was announced by the General Electric R&D Center on November 30, 1988. Harris Semiconductor Corporation has developed two generations of $p$-MCTs. Gen-1 $p$-MCTs are available at 65 A/1000 V and 75 A/600 V with peak controllable current of 120 A. Gen-2 $p$-MCTs are being developed at similar current and voltage ratings, with much improved turn-on capability and switching speed. The reason for developing a $p$-MCT is the fact that the current density that can be turned off is two or three times higher than that of an $n$-MCT; but $n$-MCTs are the ones needed for many practical applications.

The advantage of an MCT over IGBT is its low forward voltage drop. $n$-type MCTs will be expected to have a similar forward voltage drop, but with an improved reverse bias safe operating area and switching speed. MCTs have relatively low switching times and storage time. The MCT is capable of high current densities and blocking voltages in both directions. Since the power gain of an MCT is extremely high, it could be driven directly from logic gates. An MCT has high $di/dt$ (of the order of 2500 A/µs) and high $dv/dt$ (of the order of 20,000 V/µs) capability.

The MCT, because of its superior characteristics, shows a tremendous possibility for applications such as motor drives, uninterrupted power supplies, static VAR compensators, and high power active power line conditioners.

The current and future power semiconductor devices developmental direction is shown in Fig. 1.8. High-temperature operation capability and low forward voltage drop operation can be obtained if silicon is replaced by silicon carbide material for producing power devices. The silicon carbide has a higher band gap than silicon. Hence, higher breakdown voltage devices could be developed. Silicon carbide devices have excellent switching characteristics and stable blocking voltages at higher temperatures. But the silicon carbide devices are still in the very early stages of development.
1.2 Diodes

Sohail Anwar

Power diodes play an important role in power electronics circuits. They are mainly used as uncontrolled rectifiers to convert single-phase or three-phase AC voltage to DC. They are also used to provide a path for the current flow in inductive loads. Typical types of semiconductor materials used to construct diodes are silicon and germanium. Power diodes are usually constructed using silicon because silicon diodes can operate at higher current and at higher junction temperatures than germanium diodes. The symbol for a semiconductor diode is given in Fig. 1.9. The terminal voltage and current are represented as $V_d$ and $I_d$, respectively. Figure 1.10 shows the structure of a diode. It has an anode (A) terminal and a cathode (K) terminal. The diode is constructed by joining together two pieces of semiconductor material—a $p$-type and an $n$-type—to form a $pn$-junction. When the anode terminal is positive with respect to the cathode terminal, the $pn$-junction becomes forward-biased and the diode conducts current with a relatively low voltage drop. When the cathode terminal is positive with respect to the anode terminal, the $pn$-junction becomes reverse-biased and the current flow is blocked. The arrow on the diode symbol in Fig. 1.9 shows the direction of conventional current flow when the diode conducts.
Characteristics

The voltage-current characteristics of a diode are shown in Fig. 1.11. In the forward region, the diode starts conducting as the anode voltage is increased with respect to the cathode. The voltage where the current starts to increase rapidly is called the knee voltage of the diode. For a silicon diode, the knee voltage is approximately 0.7 V. Above the knee voltage, small increases in the diode voltage produce large increases in the diode current. If the diode current is too large, excessive heat will be generated, which can destroy the diode. When the diode is reverse-biased, diode current is very small for all values of reverse voltage less than the diode breakdown voltage. At breakdown, the diode current increases rapidly for small increases in diode voltage.

Principal Ratings for Diodes

Figures 1.12 and 1.13 show typical data sheets for power diodes.

Maximum Average Forward Current

The maximum average forward current ($I_{f(avg)_{max}}$) is the current a diode can safely handle when forward biased. Power diodes are available in ratings from a few amperes to several hundred amperes. For example, the power diode $D_6$ described in the data specification sheet (Fig. 1.12) can handle up to 6 A in the forward direction when used as a rectifier.

Peak Inverse Voltage

The peak inverse voltage (PIV) of a diode is the maximum reverse voltage that can be connected across a diode without breakdown. The peak inverse voltage is also called peak reverse voltage or reverse breakdown voltage. The PIV ratings of power diodes extend from a few volts to several thousand volts. For example, the power diode $D_6$ has a PIV rating of up to 1600 V, as shown in Fig. 1.12.
Rectifier Diode
D6

Technical Data
Typical applications: All purpose high power rectifier diodes, Non-controllable and half controlled rectifiers. Free-wheeling diodes.

<table>
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<th>Type No.</th>
<th>$V_{RMM}$ (Volts)</th>
<th>$V_{RSM}$ (Volts)</th>
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<tr>
<td>D6/02</td>
<td>200</td>
<td>300</td>
</tr>
<tr>
<td>D6/04</td>
<td>400</td>
<td>500</td>
</tr>
<tr>
<td>D6/08</td>
<td>800</td>
<td>900</td>
</tr>
<tr>
<td>D6/12</td>
<td>1200</td>
<td>1300</td>
</tr>
<tr>
<td>D6/16</td>
<td>1600</td>
<td>1700</td>
</tr>
</tbody>
</table>

Features
- Reverse voltage up to 1600V.
- Hermetic glass to metal seal
- C: Cathode to stud
- A: Anode to stud

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Conditions</th>
<th>Values</th>
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<tr>
<td>$I_{RMM}$</td>
<td>$\sin 180^\circ$; $T_{case} = 130^\circ C$</td>
<td>6 A</td>
</tr>
<tr>
<td>$I_{RSM}$</td>
<td>$T_{vj} = 25^\circ C$; $10 , ms$</td>
<td>190 A</td>
</tr>
<tr>
<td></td>
<td>$T_{vj} = 180^\circ C$; $10 , ms$</td>
<td>160 A</td>
</tr>
<tr>
<td>$P_t$</td>
<td>$T_{vj} = 25^\circ C$</td>
<td>180 A$^2$s</td>
</tr>
<tr>
<td></td>
<td>$T_{vj} = 180^\circ C$</td>
<td>130 A$^2$s</td>
</tr>
<tr>
<td>$I_{RSM}$</td>
<td>$T_{vj} = 180^\circ C$</td>
<td>2.2 mA max</td>
</tr>
<tr>
<td>$V_f$</td>
<td>$T_{vj} = 25^\circ C$; $I_f = 15$ A</td>
<td>1.25 V max</td>
</tr>
<tr>
<td>$V_a$</td>
<td>$T_{vj} = 180^\circ C$</td>
<td>0.85 V</td>
</tr>
<tr>
<td>$R_a$</td>
<td>$T_{vj} = 180^\circ C$</td>
<td>25 m$\Omega$</td>
</tr>
<tr>
<td>$R_{exp}$</td>
<td></td>
<td>3.8 $^\circ$C/W</td>
</tr>
<tr>
<td>$R_{f(n)}$</td>
<td></td>
<td>1.0 $^\circ$C/W</td>
</tr>
<tr>
<td>$T_d$</td>
<td></td>
<td>180 $^\circ$C</td>
</tr>
<tr>
<td>$T_{es}$</td>
<td></td>
<td>-40......+ 180 $^\circ$C</td>
</tr>
<tr>
<td>Mounting torque</td>
<td>SI units</td>
<td>2 Nm</td>
</tr>
<tr>
<td>Weight</td>
<td>Approx</td>
<td>20 g</td>
</tr>
<tr>
<td>Case outline</td>
<td></td>
<td>C/P</td>
</tr>
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</table>

FIGURE 1.12 Diode data sheet—ratings. (From USHA, India. With permission.)
FIGURE 1.13  Diode data sheet—characteristic curves.
Maximum Surge Current

The $I_{FSM}$ (forward surge maximum) rating is the maximum current that the diode can handle as an occasional transient or from a circuit fault. The $I_{FSM}$ rating for the power diode $D_6$ is up to 190 A, as shown in Fig. 1.12.

Maximum Junction Temperature

This parameter defines the maximum junction temperature that a diode can withstand without failure. The maximum junction temperature for the power diode $D_6$ is 180°C.

Rectifier Circuits

Rectifier circuits produce a DC voltage or current from an AC source. The diode is an essential component of these circuits. Figure 1.14 shows a half-wave rectifier circuit using a diode. During the positive half cycle of the source voltage, the diode is forward-biased and conducts for $v_i(t) > E_f$. The value of $E_f$ for germanium is 0.2 V and for silicon it is 0.7 V. During the negative half cycle of $v_i(t)$, the diode is reverse-biased and does not conduct. The voltage $v_L(t)$ across the load $R_L$ is shown in Fig. 1.15.

The half-wave rectifier circuit produces a pulsating direct current that uses only the positive half cycle of the source voltage. The full-wave rectifier shown in Fig. 1.16 uses both half cycles of source voltage. During the positive half cycle of $v_i(t)$, diodes $D_1$ and $D_2$ are forward-biased and conduct. Diodes $D_3$ and $D_4$ are reverse-biased and do not conduct. During the negative half cycle of $v_i(t)$, diodes $D_1$ and $D_2$ are reverse-biased and do not conduct, whereas diodes $D_3$ and $D_4$ are forward-biased and conduct. The voltage $v_L(t)$ across the load $R_L$ is shown in Fig. 1.17.
Testing a Power Diode

An ohmmeter can be used to test power diodes. The ohmmeter is connected so that the diode is forward-biased. This should give a low resistance reading. Reversing the ohmmeter leads should give a very high resistance or even an infinite reading. A very low resistance reading in both directions indicates a shorted diode. A high resistance reading in both directions indicates an open diode.

Protection of Power Diodes

A power diode must be protected against over current, over voltage, and transients. When a diode is reverse-biased, it acts like an open circuit. If the reverse bias voltage exceeds the breakdown voltage, a large current flow results. With this high voltage and large current, power dissipation at the diode junction may exceed its maximum value, destroying the diode. For the diode protection, it is a usual practice to choose a diode with a peak reverse voltage rating that is 1.2 times higher than the expected voltage during normal operating conditions.

Current ratings for diodes are based on the maximum junction temperatures. As a safety precaution, it is recommended that the diode current be kept below this rated value. Electrical transients can cause higher-than-normal voltages across a diode. To protect a diode from the transients, an RC series circuit may be connected across the diode to reduce the rate of change of voltage.
1.3 Schottky Diodes

Sohail Anwar

Bonding a metal, such as aluminum or platinum, to n-type silicon forms a Schottky diode. The Schottky diode is often used in integrated circuits for high-speed switching applications. An example of a high-speed switching application is a detector at microwave frequencies. The Schottky diode has a voltage-current characteristic similar to that of a silicon pn-junction diode. The Schottky is a subgroup of the TTL family and is designed to reduce the propagation delay time of the standard TTL IC chips. The construction of the Schottky diode is shown in Fig. 1.18a, and its symbol is shown in Fig. 1.18b.

Characteristics

The low-noise characteristics of the Schottky diode make it ideal for application in power monitors of low-level radio frequency, detectors for high frequency, and Doppler radar mixers. One of the main advantages of the Schottky barrier diode is its low forward voltage drop compared with that of a silicon diode. In the reverse direction, both the breakdown voltage and the capacitance of a Schottky barrier diode behave very much like those of a one-sided step junction. In the one-sided step junction, the doping level of the semiconductor determines the breakdown voltage. Because of the finite radius at the edges of the diode and because of its sensitivity to surface cleanliness, the breakdown voltage is always somewhat lower than theoretical predictions.

Data Specifications

The data specification sheet for a DSS 20-0015B power Schottky diode is provided as an example in Figs. 1.19 and 1.20. Specifications will vary depending on the application and model of Schottky diode.

Testing of Schottky Diodes

Two ways of testing the diodes use either a voltmeter or a digital multimeter. The voltmeter should be set to the low resistance scale. A single diode or rectifier should read a low resistance, typically, 2/3 scale from the resistance in the forward direction. In the reverse direction, the resistance should be nearly infinite. It should not read near 0 Ω in the shorted or open directions. The diode will result in a higher
### Power Schottky Rectifier

#### Preliminary Data

<table>
<thead>
<tr>
<th>$V_{RDS}$</th>
<th>$V_{RRM}$</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>15</td>
<td>DSS 20-0015B</td>
</tr>
</tbody>
</table>

#### Features
- International standard package
- Very low $V_F$
- Extremely low switching losses
- Low $I_{RM}$ values
- Epoxy meets UL 94V-0
- TO-220 AC

#### Applications
- Rectifiers in switch mode power supplies (SMPS)
- Free wheeling diode in low voltage converters

#### Advantages
- High reliability circuit operation
- Low voltage peaks for reduced protection circuits
- Low noise switching
- Low losses

#### Dimensions
- See outlines.pdf

#### Pulse Test
- Pulse Width = 5 ms, Duty Cycle < 2.0 %

Data according to IEC 60747 and per diode unless otherwise specified.

IXYS reserves the right to change limits, Conditions and dimensions.

---

**FIGURE 1.19**  Data specification sheet for a DSS 20-00105B power Schottky diode (front). (Courtesy of IXYS.)
scale reading of resistance as a result of its lower voltage drop. What is being measured is the resistance at a particular low current point; it is not the actual resistance in a power rectifier circuit.

The digital multimeter will usually have a diode test mode. When using this mode, a silicon diode should read between 0.5 to 0.8 V in the forward direction and open in the reverse direction. A germanium diode will be in the range of 0.2 to 0.4 V in the forward direction. By using the normal resistance range, these diodes will usually show open for any semiconductor junction since the voltmeter does not apply enough voltage to reach the value of the forward drop.
1.4 Thyristors

Sohail Anwar

Thyristors are four-layer \textit{pnpn} power semiconductor devices. These devices switch between conducting and nonconducting states in response to a control signal. Thyristors are used in timing circuits, AC motor speed control, light dimmers, and switching circuits. Small thyristors are also used as pulse sources for large thyristors. The thyristor family includes the silicon-controlled rectifier (SCR), the DIAC, the Triac, the silicon-controlled switch (SCS), and the gate turn-off thyristor (GTO).

The Basics of Silicon-Controlled Rectifiers (SCR)

The SCR is the most commonly used electrical power controller. An SCR is sometimes called a \textit{pnpn} diode because it conducts electrical current in only one direction. Figure 1.21a shows the SCR symbol. It has three terminals: the anode (A), the cathode (K), and the gate (G). The anode and the cathode are the power terminals and the gate is the control terminal. The structure of an SCR is shown in Fig. 1.21b.

When the SCR is forward-biased, that is, when the anode of an SCR is made more positive with respect to the cathode, the two outermost \textit{pn}-junctions are forward-biased. The middle \textit{pn}-junction is reverse-biased and the current cannot flow. If a small gate current is now applied, it forward-biases the middle \textit{pn}-junction and allows a much larger current to flow through the device. The SCR stays ON even if the gate current is removed. SCR shutoff occurs only when the anode current becomes less than a level called the holding current (\textit{IH}).

Characteristics

The volt-ampere characteristic of an SCR is shown in Fig. 1.22. If the forward bias is increased to the forward breakover voltage, \textit{V_{FBO}}, the SCR turns ON. The value of forward breakover voltage is controlled by the gate current \textit{I_g}. If the gate-cathode \textit{pn}-junction is forward-biased, the SCR is turned ON at a lower breakover voltage than with the gate open. As shown in Fig. 1.22, the breakover voltage decreases with an increase in the gate current. At a low gate current, the SCR turns ON at a lower forward anode voltage. At a higher gate current, the SCR turns ON at a still lower value of forward anode voltage.

When the SCR is reverse-biased, there is a small reverse leakage current (\textit{I_k}). If the reverse bias is increased until the voltage reaches the reverse breakdown voltage (\textit{V_{BRK}}), the reverse current will increase sharply. If the current is not limited to a safe value, the SCR may be destroyed.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{fig1.21}
\caption{(a) The SCR symbol; (b) the SCR structure.}
\end{figure}
If an SCR is forward-biased and a gate signal is applied, the device turns ON. Once the anode current is above $I_{th}$, the gate loses control. The only way to turn OFF the SCR is to make the anode terminal negative with respect to the cathode or to decrease the anode current below $I_{th}$. The process of SCR turnoff is called commutation. Figure 1.23 shows an SCR commutation circuit. This type of commutation method is called

**FIGURE 1.22** SCR characteristics.

**FIGURE 1.23** An SCR turn-off circuit.

**SCR Turn-Off Circuits**

If an SCR is forward-biased and a gate signal is applied, the device turns ON. Once the anode current is above $I_{th}$, the gate loses control. The only way to turn OFF the SCR is to make the anode terminal negative with respect to the cathode or to decrease the anode current below $I_{th}$. The process of SCR turnoff is called commutation. Figure 1.23 shows an SCR commutation circuit. This type of commutation method is called
AC line commutation. The load current $I_L$ flows during the positive half cycle of the source voltage. The SCR is reverse-biased during the negative half cycle of the source voltage. With a zero gate current, the SCR will turn OFF if the turn-off time of the SCR is less than the duration of the half cycle.

**SCR Ratings**

A data sheet for a typical thyristor follows this section and includes the following information:

*Surge Current Rating ($I_{FM}$)—The surge current rating ($I_{FM}$) of an SCR is the peak anode current an SCR can handle for a short duration.*

*Latching Current ($I_L$)—A minimum anode current must flow through the SCR in order for it to stay ON initially after the gate signal is removed. This current is called the latching current ($I_L$).*

*Holding Current ($I_H$)—After the SCR is latched on, a certain minimum value of anode current is needed to maintain conduction. If the anode current is reduced below this minimum value, the SCR will turn OFF.*

*Peak Repetitive Reverse Voltage ($V_{RRM}$)—The maximum instantaneous voltage that an SCR can withstand, without breakdown, in the reverse direction.*

*Peak Repetitive Forward Blocking Voltage ($V_{DRM}$)—The maximum instantaneous voltage that the SCR can block in the forward direction. If the $V_{DRM}$ rating is exceeded, the SCR will conduct without a gate voltage.*

*Nonrepetitive Peak Reverse Voltage ($V_{RSM}$)—The maximum transient reverse voltage that the SCR can withstand.*

*Maximum Gate Trigger Current ($I_{GTM}$)—The maximum DC gate current allowed to turn the SCR ON.*

*Minimum Gate Trigger Voltage ($V_{GT}$)—The minimum DC gate-to-cathode voltage required to trigger the SCR.*

*Minimum Gate Trigger Current ($I_{GT}$)—The minimum DC gate current necessary to turn the SCR ON.*

**The DIAC**

A DIAC is a three-layer, low-voltage, low-current semiconductor switch. The DIAC symbol is shown in Fig. 1.24a. The DIAC structure is shown in Fig. 1.24b. The DIAC can be switched from the OFF to the ON state for either polarity of applied voltage.

The volt-ampere characteristic of a DIAC is shown in Fig. 1.25. When Anode 1 is made more positive than Anode 2, a small leakage current flows until the breakover voltage $V_{BO}$ is reached. Beyond $V_{BO}$, the

![DIAC Symbol and Structure](image-url)

**FIGURE 1.24** (a) The DIAC symbol; (b) the DIAC structure.
DIAC will conduct. When Anode 2 is made more positive relative to Anode 1, a similar phenomenon occurs. The breakover voltages for the DIAC are almost the same in magnitude in either direction. DIACs are commonly used to trigger larger thyristors such as SCRs and Triacs.

The Triac

The Triac is a three-terminal semiconductor switch. It is triggered into conduction in both the forward and the reverse directions by a gate signal in a manner similar to the action of an SCR. The Triac symbol is shown in Fig. 1.26a and the Triac structure is shown in Fig. 1.26b.

The volt-ampere characteristic of the Triac is shown in Fig. 1.27. The breakover voltage of the Triac can be controlled by the application of a positive or negative signal to the gate. As the magnitude of the gate signal increases, the breakover voltage decreases. Once the Triac is in the ON state, the gate signal can be removed and the Triac will remain ON until the main current falls below the holding current ($I_{th}$) value.

The Silicon-Controlled Switch

The SCS is a four-layer $pnpn$ device. The SCS symbol is shown in Fig. 1.28a and the SCS structure is shown in Fig. 1.28b. The SCS has two gates labeled as the anode gate (AG) and the cathode gate (KG). An SCS can be turned ON by the application of a negative gate pulse at the anode gate. When the SCS is in the ON state, it can be turned OFF by the application of a positive pulse at the anode gate or a negative pulse at the cathode gate.
The Gate Turn-Off Thyristor

The GTO is a power semiconductor switch that turns ON by a positive gate signal. It can be turned OFF by a negative gate signal. The GTO symbol is shown in Fig. 1.29a and the GTO structure is shown in Fig. 1.29b. The GTO voltage and current ratings are lower than those of SCRs. The GTO turn-off time is lower than that of SCR. The turn-on time is the same as that of an SCR.

Data Sheet for a Typical Thyristor

Figures 1.30 to 1.35 are the data sheets for a typical thyristor.
**Phils Semiconductors**

**Thyrists**

**BT151S series**

**BT151M series**

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**GENERAL DESCRIPTION**

Passivated thyristors in a plastic envelope, suitable for surface mounting, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

---

**QUICK REFERENCE DATA**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MAX. BT151S (or BT151M)</th>
<th>MAX. 500R</th>
<th>MAX. 650R</th>
<th>MAX. 800R</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DM}</td>
<td>Repetitive peak off-state voltages</td>
<td>7.5</td>
<td>7.5</td>
<td>7.5</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>I_{PM}</td>
<td>Average on-state current</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>I_{RMS}</td>
<td>RMS on-state current</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>I_{PM}</td>
<td>Non-repetitive peak on-state current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
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---

**PINNING - SOT428**

<table>
<thead>
<tr>
<th>PIN NUMBER</th>
<th>PIN</th>
<th>Standard Number</th>
<th>Alternative Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>cathode</td>
<td>gate</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>anode</td>
<td>anode</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>gate</td>
<td>anode</td>
<td></td>
</tr>
<tr>
<td>tab</td>
<td>anode</td>
<td>anode</td>
<td></td>
</tr>
</tbody>
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**PIN CONFIGURATION**

**SYMBOL**

---

**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134).

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN. BT151S (or BT151M)</th>
<th>MAX. 500R</th>
<th>MAX. 650R</th>
<th>MAX. 800R</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DM}</td>
<td>Repetitive peak off-state voltages</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{PM}</td>
<td>Average on-state current</td>
<td>half sine wave; T_{th} &lt; 103 °C</td>
<td>7.5</td>
<td>A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{RMS}</td>
<td>RMS on-state current</td>
<td>all conduction angles</td>
<td>12</td>
<td>A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{PM}</td>
<td>Non-repetitive peak on-state current</td>
<td>half sine wave; T_{th} = 25 °C prior to surge</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[\int I(t) dt]</td>
<td>ft for fusing</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[\frac{dI(t)}{dt}]</td>
<td>Repetitive rate of rise of on-state current after triggering</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{GM}</td>
<td>Peak gate current</td>
<td></td>
<td>2</td>
<td>A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{GM}</td>
<td>Peak gate voltage</td>
<td></td>
<td>5</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{RGM}</td>
<td>Peak reverse gate voltage</td>
<td></td>
<td>5</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P_{GM}</td>
<td>Peak gate power</td>
<td></td>
<td>5</td>
<td>W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P_{AVG}</td>
<td>Average gate power</td>
<td>over any 20 ms period</td>
<td>0.5</td>
<td>W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_{se}</td>
<td>Storage temperature</td>
<td></td>
<td>-40</td>
<td>°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_{j}</td>
<td>Operating junction temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/μs.

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Rev 1.200

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FIGURE 1.30  Page 1 of a data sheet for a typical thyristor. (From Philips Semiconductors. With permission.)
THERMAL RESISTANCES

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{jeb}</td>
<td>Thermal resistance junction to mounting base</td>
<td>pcb (FR4 mounted; footprint as in Fig.14)</td>
<td>-</td>
<td>75</td>
<td>-</td>
<td>KW</td>
</tr>
<tr>
<td>R_{ja}</td>
<td>Thermal resistance junction to ambient</td>
<td></td>
<td>-</td>
<td>-</td>
<td>1.8</td>
<td>KW</td>
</tr>
</tbody>
</table>

STATIC CHARACTERISTICS

\( T_J = 25 ^\circ \text{C} \) unless otherwise stated

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{GT}</td>
<td>Gate trigger current</td>
<td>( V_S = 12 \text{ V}; I_T = 0.1 \text{ A} )</td>
<td>-</td>
<td>2</td>
<td>15</td>
<td>mA</td>
</tr>
<tr>
<td>I_C</td>
<td>Latching current</td>
<td>( V_S = 12 \text{ V}; I_{GT} = 0.1 \text{ A} )</td>
<td>-</td>
<td>10</td>
<td>40</td>
<td>mA</td>
</tr>
<tr>
<td>I_H</td>
<td>Holding current</td>
<td>( V_S = 12 \text{ V}; I_{GT} = 0.1 \text{ A} )</td>
<td>-</td>
<td>7</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td>V_{GT}</td>
<td>On-state voltage</td>
<td>( I_T = 2.3 \text{ A} )</td>
<td>-</td>
<td>1.4</td>
<td>1.75</td>
<td>V</td>
</tr>
<tr>
<td>V_{GT}</td>
<td>Gate trigger voltage</td>
<td>( I_T = 0.1 \text{ A} )</td>
<td>-</td>
<td>0.6</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>I_{ON}, I_{IN}</td>
<td>Off-state leakage current</td>
<td>( V_S = V_{GMIN} ); ( I_T = 0.1 \text{ A} ); ( T_J = 125 ^\circ \text{C} )</td>
<td>0.25</td>
<td>0.4</td>
<td>-</td>
<td>V</td>
</tr>
</tbody>
</table>

DYNAMIC CHARACTERISTICS

\( T_J = 25 ^\circ \text{C} \) unless otherwise stated

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \frac{dV}{dt} )</td>
<td>Critical rate of rise of off-state voltage</td>
<td>( V_{ON} = 67 % V_{GMIN} ); ( T_J = 125 ^\circ \text{C} ); exponential waveform; ( \frac{dV}{dt} = \text{ gate open circuit} ); ( R_{OK} = 100 \text{ ohm} )</td>
<td>-</td>
<td>50</td>
<td>130</td>
<td>V/\mu s</td>
</tr>
<tr>
<td>t_A</td>
<td>Gate controlled turn-on time</td>
<td>( I_{ON} = 40 \text{ A} ); ( V_{S} = V_{GMIN} ); ( I_T = 0.1 \text{ A} ); ( \frac{dI_{GT}}{dt} = 5 \text{ A/\mu s} )</td>
<td>-</td>
<td>200</td>
<td>1000</td>
<td>-</td>
</tr>
<tr>
<td>t_T</td>
<td>Circuit commutated turn-off time</td>
<td>( V_S = 67 % V_{GMIN} ); ( T_J = 125 ^\circ \text{C} ); ( I_{ON} = 20 \text{ A} ); ( V_S = 25 \text{ V} ); ( \frac{dI_{GT}}{dt} = 30 \text{ A/\mu s} ); ( \frac{dV}{dt} = 50 \text{ V/\mu s} ); ( R_{OK} = 100 \text{ ohm} )</td>
<td>-</td>
<td>70</td>
<td>-</td>
<td>\mu s</td>
</tr>
</tbody>
</table>

FIGURE 1.31  Page 2 of a data sheet for a typical thyristor. (From Philips Semiconductors. With permission.)
FIGURE 1.32  Page 3 of a data sheet for a typical thyristor. (From Philips Semiconductors. With permission.)
FIGURE 1.33  Page 4 of a data sheet for a typical thyristor. (From Philips Semiconductors. With permission.)
FIGURE 1.34  Page 5 of a data sheet for a typical thyristor. (From Philips Semiconductors. With permission.)
Power Bipolar Junction Transistors

Sohail Anwar

Power bipolar junction transistors (BJTs) play a vital role in power circuits. Like most other power devices, power transistors are generally constructed using silicon. The use of silicon allows operation of a BJT at higher currents and junction temperatures, which leads to the use of power transistors in AC applications where ranges of up to several hundred kilowatts are essential.

The power transistor is part of a family of three-layer devices. The three layers or terminals of a transistor are the base, the collector, and the emitter. Effectively, the transistor is equivalent to having two pn-diode junctions stacked in opposite directions to each other. The two types of a transistor are termed npn and pnp. The npn-type transistor has a higher current-to-voltage rating than the pnp and is preferred for most power conversion applications. The easiest way to distinguish an npn-type transistor from a pnp-type is by virtue of the schematic or circuit symbol. The pnp type has an arrowhead on the emitter that points toward the base. Figure 1.36 shows the structure and the symbol of a pnp-type transistor. The npn-type transistor has an arrowhead pointing away from the base. Figure 1.37 shows the structure and the symbol of an npn-type transistor.

When used as a switch, the transistor controls the power from the source to the load by supplying sufficient base current. This small current from the driving circuit through the base–emitter, which must be maintained, turns on the collector—emitter path. Removing the current from the base–emitter path and making the base voltage slightly negative turns off the switch. Even though the base–emitter path may only utilize a small amount of current, the collector–emitter path is capable of carrying a much higher current.
The volt-ampere characteristics of a BJT are shown in Fig. 1.38. Power transistors have exceptional characteristics as an ideal switch and they are primarily used as switches. In this type of application, they make use of the common emitter connection shown in Fig. 1.39. The three regions of operation for a transistor that must be taken into consideration are the cutoff, saturation, and the active region. When the base current \( I_B \) is zero, the collector current \( I_C \) is insignificant and the transistor is driven into the cutoff region. The transistor is now in the OFF state. The collector–base and base–emitter junctions are reverse-biased in the cutoff region or OFF state, and the transistor behaves as an open switch. The base current \( I_B \) determines the saturation current. This occurs when the base current is sufficient to drive the transistor into saturation. During saturation, both junctions are forward-biased and the transistor acts like a closed switch. The saturation voltage increases with an increase in current and is normally between 0.5 to 2.5 V. The active region of the transistor is mainly used for amplifier applications and should be avoided for switching operation. In the active region, the collector–base junction is reverse-biased and the base–emitter junction is forward-biased.
BJT Biasing

When a transistor is used as a switch, the control circuit provides the necessary base current. The current of the base determines the ON or OFF state of the transistor switch. The collector and the emitter of the transistor form the power terminals of the switch.

The DC load line represents all of the possible operating points of a transistor and is shown in Fig. 1.40. The operating point is where the load line and the base current intersect and is determined by the values of $V_{CC}$ and $R_C$.

In the ON state, the ideal operating point occurs when the collector current $I_C$ is equal to $V_{CC}/R_C$ and $V_{CE}$ is zero. The actual operating point occurs when the load line intersects the base current at the saturation point. This occurs when the base current equals the saturation current or $I_B = I_{B(sat)}$. At this point, the collector current is maximum and the transistor has a small voltage drop across the collector–emitter terminals called the saturation voltage $V_{CE(sat)}$.

In the OFF state, or cutoff point, the ideal operating point occurs when the collector current $I_C$ is zero and the collector–emitter voltage $V_{CE}$ is equal to the supply voltage $V_{CC}$. The actual operating point, in the OFF state, occurs when the load line intersects the base current ($I_B = 0$). At the cutoff point, the collector current is the leakage current. By applying Kirchoff’s voltage law around the output loop, the collector–emitter voltage ($V_{CE}$) can be found.

The operating points between the saturation and cutoff constitute the active region. When operating in the active region, high power dissipation occurs due to the relatively high values of collector current.
I<sub>C</sub> and collector–emitter voltage V<sub>CE</sub>. For satisfactory operation, a slightly higher than minimum base current will ensure a saturated ON state and will result in reduced turn-on time and power dissipation.

**BJT Power Losses**

The four types of transistor power losses are the ON-state and OFF-state losses and turn-ON and turn-OFF switching loss. OFF-state transistor losses are much lower than ON-state losses since the leakage current of the device is within a few milliamps. Essentially, when a transistor is in the off state, whatever the value of collector–emitter voltage, there is no collector current. Switching losses depend on switching frequency. The highest possible switching frequency of the transistor is limited by the losses due to the rate of switching. In other words, the higher the switching frequency, the more power loss in the transistor.

**BJT Testing**

Testing of the state of a transistors can be done with a multimeter. When a transistor is forward-biased, the base–collector and base–emitter regions should have a low resistance. When reverse-biased, the base–collector and base–emitter regions should have a high resistance. When testing the resistance between the collector and the emitter, the resistance reading should result in a much higher than forward bias base–collector and base–emitter resistance. However, faulty power transistors can appear shorted when measuring resistance across the collector and emitter, but still pass both junction tests.

**BJT Protection**

Transistors must be protected against high currents and voltages to prevent damage to the device. Since they are able to absorb very little energy before breakdown, semiconductor fuses cannot protect them. Thermal conditions are vitally important and can occur during high-frequency switching. Some of the most common types of BJT protection are overcurrent and overvoltage protection. Electronic protection techniques are also frequently used to provide needed protection for transistors.

Overcurrent protection turns the transistor OFF when the collector–emitter voltage and collector current reach a preset value. When the transistor is in the ON state, an increase in collector–emitter voltage causes an increase in the collector current and therefore an increase in junction temperature. Since the BJT has a negative temperature coefficient, the increase in temperature causes a decrease in resistance and results in an even higher collector current. This condition, called positive feedback, could eventually lead to thermal runaway and destroy the transistor. One such method of overcurrent protection limits the base current during an external fault. With the base current limited, the device current will be limited at the saturation point, with respect to the base current, and the device will hold some value of the voltage. This feature turns the transistor off without being damaged and is used for providing

![DC load line](image-url)
General Description

The LM195/LM395 are fast, monolithic power integrated circuits with complete overload protection. These devices, which act as high gain power transistors, have included on the chip, current limiting, power limiting, and thermal overload protection making them virtually impossible to destroy from any type of overload. In the standard TO-3 transistor power package, the LM195 will deliver load currents in excess of 1.0A and can switch 40V in 500 ns.

The inclusion of thermal limiting, a feature not easily available in discrete designs, provides virtually absolute protection against overload. Excessive power dissipation or inadequate heat sinking causes the thermal limiting circuitry to turn off the device preventing excessive heating.

The LM195 offers a significant increase in reliability as well as simplifying power circuitry. In some applications, where protection is unusually difficult, such as switching regulators, lamp or solenoid drivers where normal power dissipation is low, the LM195 is especially advantageous.

The LM195 is easy to use and only a few precautions need be observed. Excessive collector to emitter voltage can destroy the LM195 as with any power transistor. When the device is used as an emitter follower with low source impedance, it is necessary to insert a 5.0k resistor in series with the base lead to prevent possible emitter follower oscillations. Although the device is usually stable as an emitter follower, the resistor eliminates the possibility of trouble without degrading performance. Finally, since it has good high frequency response, supply bypassing is recommended.

For low-power applications (under 100 mA), refer to the LP395 Ultra Reliable Power Transistor.

The LM195/LM395 are available in the standard TO-3, Kovar TO-5, and TO-220 packages. The LM195 is rated for operation from -55 C to +150 C and the LM395 from 0 C to +125 C.

Features

- Internal thermal limiting
- Greater than 1.0A output current
- 3.0 A typical base current
- 500 ns switching time
- 2.0V saturation
- Base can be driven up to 40V without damage
- Directly interfaces with CMOS or TTL
- 100% electrical burn-in

Simplified Circuit

![Simplified Circuit Diagram](image)

FIGURE 1.41 Typical data sheet for a power transistor (page 1). (From National Semiconductor. With permission.)
FIGURE 1.42 Typical data sheet for a power transistor (page 2). (From National Semiconductor. With permission.)
### Absolute Maximum Ratings (Note 1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LM195</th>
<th>LM395</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector to Emitter Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LM195</td>
<td>42 V</td>
<td>20 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LM395</td>
<td>36 V</td>
<td>20 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector to Base Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LM195</td>
<td>42 V</td>
<td>20 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LM395</td>
<td>36 V</td>
<td>20 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Base to Emitter Voltage (Forward)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LM195</td>
<td>42 V</td>
<td>20 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LM395</td>
<td>36 V</td>
<td>20 V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Collectors to Emitter Voltage

| Base to Emitter Voltage (Reverse)        |                                 |       |       | 260 C     |
| Collector Current                        |                                 | 0     |       |           |
| Power Dissipation                        |                                 |       | 0     |           |
| Operating Temperature Range              |                                 |       |       |           |
| LM195                                    | 55 C to +150 C                  |       |       |           |
| LM395                                    | 0 C to +125 C                   |       |       |           |
| Storage Temperature Range                |                                 |       |       |           |
| LM195                                    | 65 C to +150 C                  |       |       |           |
| Lead Temperature                         |                                 |       | 260 C |           |

(Soldering, 10 sec.)

Preconditioning

100% Burn-In In Thermal Limit

#### Electrical Characteristics (Note 2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LM195</th>
<th>LM395</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-Emitter Operating Voltage</td>
<td>$I_C \leq I_C \leq I_{MAX}$</td>
<td>42</td>
<td>36</td>
<td>V</td>
</tr>
<tr>
<td>Base to Emitter Breakdown Voltage</td>
<td>$0 \leq V_{CE} \leq V_{CEMAX}$</td>
<td>42</td>
<td>36</td>
<td>V</td>
</tr>
<tr>
<td>Collector Current</td>
<td></td>
<td>1.2</td>
<td>1.2</td>
<td>A</td>
</tr>
<tr>
<td>TO-3, TO-220</td>
<td>$V_C \leq 15 V$</td>
<td>2.2</td>
<td>2.2</td>
<td>A</td>
</tr>
<tr>
<td>TO-5</td>
<td>$V_C \leq 7.0 V$</td>
<td>1.8</td>
<td>1.8</td>
<td>A</td>
</tr>
<tr>
<td>Saturation Voltage</td>
<td>$I_C = 1.0 A, T_A = 25 C$</td>
<td>1.8</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td>Base Current</td>
<td>$0 \leq I_C \leq I_{MAX}$</td>
<td>3.0</td>
<td>3.0</td>
<td>A</td>
</tr>
<tr>
<td>$0 \leq V_{CE} \leq V_{CEMAX}$</td>
<td></td>
<td>5.0</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Quiescent Current ($I_Q$)</td>
<td>$V_{th} = 0$</td>
<td>2.0</td>
<td>2.0</td>
<td>mA</td>
</tr>
<tr>
<td>$0 \leq V_{CE} \leq V_{CEMAX}$</td>
<td></td>
<td>5.0</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Base to Emitter Voltage (Note 3)</td>
<td>$I_C = 1.0 A, T_A = +25 C$</td>
<td>0.9</td>
<td>0.9</td>
<td>V</td>
</tr>
<tr>
<td>Switching Time</td>
<td>$V_{CE} = 36 V, R_L = 36 \Omega, T_A = +25 C$</td>
<td>500</td>
<td>500</td>
<td>ns</td>
</tr>
<tr>
<td>Thermal Resistance Junction to Case</td>
<td>TO-3 Package (K)</td>
<td>2.3</td>
<td>3.0</td>
<td>C/W</td>
</tr>
<tr>
<td></td>
<td>TO-5 Package (H)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TO-220 Package (T)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: Unless otherwise specified, these specifications apply for 55 C $\leq T_A \leq +150 C$ for the LM195 and 0 C $\leq +125 C$ for the LM395.

Note 3: Without a heat sink, the thermal resistance of the TO-5 package is about +150 C/W, while that of the TO-3 package is +35 C/W.

Note 4: Selected devices with higher breakdown available.

Note 5: Refer to RETS195H and RETS195K drawings of military LM195H and LM195K versions for specifications.

FIGURE 1.43  Typical data sheet for a power transistor (page 3). (From National Semiconductor. With permission.)
FIGURE 1.44  Typical data sheet for a power transistor (page 4). (From National Semiconductor. With permission.)
Typical Performance Characteristics (for K and T Packages) (Continued)

**10V Transfer Function**

![10V Transfer Function](image1)

**36V Transfer Function**

![36V Transfer Function](image2)

**Transconductance**

![Transconductance](image3)

**Small Signal Frequency Response**

![Small Signal Frequency Response](image4)

FIGURE 1.45  Typical data sheet for a power transistor (page 5). (From National Semiconductor. With permission.)
FIGURE 1.46  Typical data sheet for a power transistor (page 6). (From National Semiconductor. With permission.)
Typical Applications

1.0 Amp Voltage Follower

Power PNP

Time Delay

1.0 MHz Oscillator

* Solid Tantalum

* Protects against excessive base drive

** Needed for stability

FIGURE 1.47  Typical data sheet for a power transistor (page 7). (From National Semiconductor. With permission.)
Typical Applications (Continued)

1.0 Amp Negative Regulator

1.0 Amp Positive Voltage Regulator

FIGURE 1.48  Typical data sheet for a power transistor (page 8). (From National Semiconductor. With permission.)
**Typical Applications (Continued)**

- **Fast Optically Isolated Switch**
- **Optically Isolated Power Transistor**
- **CMOS or TTL Lamp Interface**
- **Two Terminal Current Limiter**
- **40V Switch**
- **6.0V Shunt Regulator with Crowbar**
- **Two Terminal 100 mA Current Regulator**

*Drive Voltage 0V to $\geq 10V \leq 42V$*

---

**FIGURE 1.49** Typical data sheet for a power transistor (page 9). (From National Semiconductor. With permission.)
Typical Applications (Continued)

**Low Level Power Switch**

- Input: 12V
- $R_2 \geq 12k$
- Turn ON = 350 mV
- Turn OFF = 200 mV

**Power One-Shot**

- $T = R_1 C$
- $R_2 = 3R_1$
- $R_2 \leq 82k$

**Emitter Follower**

- $R_1 = 5.5k$
- $R_1 \geq R_L$

**High Input Impedance AC Emitter Follower**

- $C_1 = 0.22uF$
- $R_3 = 5.0k$
- $C_2 = 50uF$

**Fast Follower**

- $R_1 = 60$
- $R_1 \geq R_L$

FIGURE 1.50  Typical data sheet for a power transistor (page 10). (From National Semiconductor. With permission.)
FIGURE 1.51  Typical data sheet for a power transistor (page 11). (From National Semiconductor. With permission.)
Physical Dimensions inches (millimeters) unless otherwise noted

TO-5 Metal Can Package
Order Number LM195H/883
NS Package Number H03B

TO-3 Metal Can Package
Order Number LM195K/883
NS Package Number K02A

FIGURE 1.52 Typical data sheet for a power transistor (page 12). (From National Semiconductor. With permission.)
protection in low power converters by limiting the current during an external fault. Other methods of overcurrent protection for more severe faults use a shorting switch, or shunt switch, in parallel with the transistor. When a fault is detected, an external circuit activates the parallel shorting switch, providing an alternate path for the fault current.

Overvoltage protection is used to protect a transistor from high voltages. When a transistor is in the OFF state, high collector-base reverse-bias voltages can cause avalanche breakdown. Avalanche breakdown occurs when the reverse voltage exceeds the reverse voltage limit of the collector–base region. High collector–base reverse-bias voltages can easily damage the transistor. One simple method to ensure overcurrent protection of a transistor is to connect an antiparallel diode across the transistor.

Most power transistors are unable to block reverse voltages in excess of 20 V. Reverse voltages can easily damage the transistor and therefore they should not be used in AC control applications without a reverse shunting diode connected between the emitter and the collector.

A typical data sheet for a power transistor is provided in Figs. 1.41 through 1.53.
1.6 MOSFETs

Vrej Barkhordarian

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the most commonly used active device in very large scale integrated (VLSI) circuits. Figure 1.54 shows the device schematic, current-voltage characteristics, transfer characteristics and device symbol for a MOSFET. It is a lateral device and though very suitable for integration into integrated circuits, it has severe limitations at high power levels. The power MOSFET design is based on the original field-effect transistor and, since its invention in the early 1970s, has gone through several evolutionary steps. The processing of power MOSFETs is very similar to that of today’s VLSI circuits although the device geometry is significantly different from the

![Schematic diagram](image)

**FIGURE 1.54** (a) Schematic diagram, (b) current-voltage characteristics, (c) transfer characteristics, and (d) device symbol for an n-channel enhancement mode MOSFET.
design used in these circuits. Power MOSFETs are commonly used as switches in power electronic applications.

The invention of the power MOSFET was partly driven by the limitations of bipolar power transistors which, until recently, were the devices of choice in power electronics applications. Although it is not possible to define absolutely the operating boundaries of a power device, we will loosely refer to the power device as any device that is capable of switching at least 1A. The bipolar power transistor is a current-controlled device and a large base drive current as high as one fifth of the collector current is required to keep the device in the on state. Also, higher reverse base drive currents are required to obtain fast turn-off. Despite the very advanced state of manufacturability and lower costs of bipolar power transistors, these limitations have made the base drive circuit design more complicated and hence more expensive. There are two further limitations to the bipolar power transistor. First, both electrons and holes contribute to conduction in BJTs. Presence of holes with their higher carrier lifetime causes the switching speed to be several orders of magnitude slower than for a power MOSFET of similar size and voltage rating. Secondly, the BJTs suffer from thermal runaway. The forward voltage drop of a BJT decreases with increasing temperature causing diversion of current to a single device when several devices are paralleled. Power MOSFETs, on the other hand, are majority carrier devices with no minority carrier injection. They are superior to the BJTs in high-frequency applications where switching power losses are important and can withstand simultaneous application of high current and voltage without undergoing destructive failure due to second breakdown. Power MOSFETs can also be paralleled easily since the forward voltage drop increases with increasing temperature, ensuring an even distribution of current among all components. However, at high breakdown voltages (>∼200V) the on-state voltage drop of the power MOSFET becomes higher than that of a similar size bipolar device with a similar voltage rating, making it more attractive to use the bipolar power transistor at the expense of worse high-frequency performance. Figure 1.55 shows the present current-voltage limitations of power MOSFETs and BJTs. New materials, structures and processing techniques are expected to push these limits out over time. A relatively new device which combines the high-frequency advantages of the MOSFET with the low on-state voltage drop of high voltage BJTs is the insulated-gate-bipolar transistor (IGBT).

**FIGURE 1.55** Current-voltage limitations of MOSFETs and BJTs.
MOSFETs used in integrated circuits are lateral devices with gate, source and drain all on the top of the device and with current flow taking place in a path parallel to the surface. Although this design lends itself to integration, it is not suitable for discrete power device applications due to large distances required between source and drain in order to maintain isolation. Having all three terminals as the upper surface makes the metallization and isolation of terminals more complicated from the processing point of view. The vertical double diffused MOSFET solves this problem by using the substrate of the device as the drain terminal. Figure 1.56 shows the schematic diagram and the circuit symbol for an n-channel power MOSFET. When a positive bias greater than the threshold voltage is applied to the gate, the silicon surface in the channel region is inverted and a current starts to flow between the source and drain. For gate voltages of less than $V_T$, no surface inversion occurs in the channel and the device remains in the off-state. The current in this device flows horizontally along the inverted channel first and then vertically between the drain and source. The term “double-diffused” refers to the two consecutive ion implantation steps using the poly as a mask. For an n-channel device, the regions formed by double implant and subsequent diffusion are first p-type to define the channel and then n-type to define the source. The p-body implant is performed in a separate step. The terms “body drift” and “body-drain” diodes are used interchangeably to denote the $p-n$ junction formed by this p-body implant and the drift region.

Figure 1.57 shows the physical origin of the parasitic components for a power MOSFET. The parasitic JFET appearing between the two body implants restricts current flow when the depletion
widths of the two adjacent body diodes extend into the drift region with increasing drain voltage. Poly line-width and the epi layer resistivity under the poly are two important design parameters for minimizing the JFET effect. The parasitic BJT can make the device susceptible to unwanted device turn-on and premature breakdown. The base resistance $R_b$ has to be minimized through careful design of the doping and distance under the source region. These two components and the parasitic resistances are discussed further in the next sections. There are several parasitic capacitances associated with the power MOSFET as shown in Fig. 1.57. $C_{GS}$ is the capacitance due to the overlap of the source and the channel regions by the polysilicon gate and is independent of applied voltage. $G_{GD}$ is made up of two parts. The first part is the capacitance associated with the overlap of the polysilicon gate and the silicon underneath in the JFET region. The second part is the capacitance associated with the depletion region immediately under the gate. $C_{GD}$ is a nonlinear function of voltage and is discussed further in the "Dynamic Characteristics" section. Finally, $C_{DS}$ is the capacitance associated with the body-drift diode and varies inversely with the square root of the drain-source bias.

There are currently two designs of power MOSFETs. These are usually referred to as the planar and the trench designs. The planar design has already been introduced in the schematics of Figs. 1.56 and 1.57. Two variations of the trench power MOSFET are shown in Fig. 1.58. The V-groove device is fabricated by etching a groove in the silicon after the double diffusion step. The use of an anisotropic etch results in the sides of the groove to be at an angle of 54.7° to the surface of the wafer. Etching stops when the groove sides, which are planes, reach each other. The gate oxide and gate poly or metallization are then grown in the groove followed by the source metallization. Current crowding at the apex of the V-groove reduces current handling capability. In a truncated V-groove design, the anisotropic etch is stopped before this point is reached. The trench technology has the advantage of higher cell density but is more difficult to manufacture compared with the planar device.

**Static Characteristics**

One of the important features of the power MOSFET is the very high input impedance which simplifies the gate drive circuitry and reduces cost. It is a voltage-controlled device with no gate current flow during operation. Figure 1.59 shows $I–V$ characteristics of an enhancement mode (normally off) power MOSFET. Data sheets contain typical graphs which can be used to determine if the device is in the fully on state or in the constant-current region for a given value of gate bias and drain current. Temperature effect on threshold voltage (about 6 mV/C reduction) and the difference between typical values of parameters and the maximums should be taken into account.
Breakdown Voltage

This is the drain voltage at which the reverse-biased body-drift diode breaks down and a significant current starts to flow between the source and drain by the avalanche multiplication process, while the gate and source are shorted together. Breakdown voltage, $BVDSS$, is normally measured at a drain current of 250 $\mu$A. For drain voltages below $BVDSS$ and with no bias on the gate, no channel is formed under the gate at the surface and the drain voltage is entirely supported by the reverse-biased body-drift $pn$ junction.

There are two related phenomena which can occur in poorly designed and processed devices. These are punch-through and reach-through.

Punch-through is observed when the depletion region on the source side of the body-drift $pn$-junction reaches the source region at drain voltages below the rated avalanche voltage of the device. This provides a current path between source and drain and causes a soft breakdown characteristic as shown in Fig. 1.60. The leakage current flowing between source and drain is denoted by $I_{DSS}$. Careful selection and optimization of the doping profile used in the fabrication of a power MOSFET is therefore very important. Figure 1.61 shows a typical diffusion profile for a power MOSFET. The surface concentration of the body diffusion and the channel length (distance between the two $pn$-junctions formed by the source diffusion and the channel diffusion) will determine whether punch-through will occur or not. There are trade-offs to be made between on-resistance $R_{DSS}$ which requires shorter channel lengths and punch-through avoidance which requires longer channel lengths. An approximate equation giving the depletion region width as a function of silicon
background doping is given by:

\[
W = \frac{4\varepsilon_r K T}{q^2 N_A} \ln \left( \frac{N_A}{n_i} \right)
\]  

(1.1)

where \(\varepsilon_r\) is semiconductor permittivity, \(K\) is Boltzmann's constant, \(T\) is temperature in K, \(q\) is electronic charge, \(N_A\) is background doping, and \(n_i\) is the intrinsic carrier density.
Also, higher channel implant dose is beneficial from the punch-through point of view since depletion width will be smaller, but the $R_{dson}$ will suffer through reduced carrier mobility. The design of the doping profile involves choosing channel and source implant doses, diffusion times and temperatures that give a designed threshold voltage while simultaneously minimizing $R_{dson}$ and $I_{DSS}$. Optimizing these performance parameters with manufacturability in mind is one of the challenges of power MOSFET design.

The reach-through phenomenon, on the other hand, occurs when the depletion region on the drift side of the body-drift $pn$-junction reaches the epilayer-substrate interface before avalanching takes place in the epi. Once the depletion edge enters the high carrier concentration substrate, a further increase in drain voltage will cause the electric field to quickly reach the critical value of $2 \times 10^{5}$ V/cm at which avalanching begins.

Other factors that affect the breakdown voltage of power MOSFETs for a given epitaxial layer include termination design, cell spacing (poly line width) and curvature of the body diode depletion region in the epi which is a function of diffusion depth. Power MOSFETs are designed such that avalanche breakdown occurs in the active area first.

**On-Resistance**

The on-state resistance of a power MOSFET is made up of several components as shown in Fig. 1.62.

\[
R_{dson} = R_{source} + R_{ch} + R_A + R_f + R_D + R_{sub} + R_{wcm}\text{l}
\]  \hspace{1cm} (1.2)

where

- $R_{source}$ = source diffusion resistance
- $R_{ch}$ = channel resistance
- $R_A$ = accumulation resistance
- $R_f$ = the “JFET” component-resistance of the region between the two body regions
- $R_D$ = drift region resistance
- $R_{sub}$ = the substrate resistance; wafers with resistivities of up to 20 mΩ-cm are used for high-voltage devices and less than 5 mΩ-cm for low-voltage devices
- $R_{wcm}$ = sum of bond wire resistance, contact resistance between the source and drain metallization and the silicon, metallization resistance, and leadframe contributions; these are normally negligible in high-voltage devices but can become significant in low-voltage devices
Figure 1.63 shows the relative importance of each of the components to \( R_{\text{dson}} \) over the voltage spectrum. As can be seen, at high voltages the \( R_{\text{dson}} \) is dominated by epi resistance and the JFET component. This component is higher in high-voltage devices due to the higher resistivity or lower background carrier concentration in the epi. At lower voltages, the \( R_{\text{dson}} \) is dominated by the channel resistance and the contributions from the metal to semiconductor contact, metallization, bond wires, and leadframe. The substrate contribution becomes more significant for lower breakdown voltage devices.

Transconductance

This parameter is a measure of the sensitivity of drain current to changes in gate-source bias and is defined as:

\[
g_{fs} = \left( \frac{\Delta I_D}{\Delta V_{gs}} \right) \quad V_{ds} \text{ constant}
\]  

(1.3)

i.e., the gradient of the \( I_d \) vs. \( V_{gs} \) graph. In the saturation region, \( g_{fs} \) is given by:

\[
g_{fs} = \mu C_{ox} \frac{W}{L} (V_{gs} - V_{th})
\]  

(1.4)

This parameter is normally quoted for a \( V_{gs} \) that gives a drain current equal to about one half of the maximum current rating value and for a \( V_{DS} \) that ensures operation in the constant current region. With mobility \( \mu \) fixed for a given semiconductor, the design parameters influencing transconductance of a MOSFET are gate width \( W \), channel length \( L \), and gate oxide thickness \( t_{ox} \) and hence \( C_{ox} \). Gate width is the total polysilicon gate perimeter of the cellular structure and increases in proportion to the active area as the cell density increases. The cell density has increased over the years from around half a million per square inch in 1980 to around 8 million for planar MOSFETs and around 12 million for the trench technology at the present time. The limiting factor for even higher cell densities is the photolithography process control and resolution which allows contacts to be made to the source metallization in the center of the cells.
Reduced channel length is beneficial to both $g_{fs}$ and on-resistance, with punch-through as a trade-off. The lower limit of this length is set by the ability to control the double-diffusion process and is around 1 to 2 $\mu$m today. Finally, reductions in gate oxide thickness give higher $C_{ox}$ and higher $g_{fs}$. The reduction in oxide thickness will reduce $V_{th}$ unless channel implant dose is increased which in turn will cause a higher $R_{dson}$. Ultimately, the lower limit of $t_{ox}$ is set by the maximum gate-source voltage rating. This is $\pm 30$ V for high-voltage devices and $\pm 20$ V for lower-voltage logic-level devices used in portable electronic applications.

Threshold Voltage
This is defined as the minimum gate electrode bias required to strongly invert the surface under the poly and form a conducting channel between the source and the drain regions. $V_{th}$ is usually measured at a drain-source current of 250 $\mu$A. A value of 2 to 4 V for high-voltage devices with thicker gate oxides and logic-compatible values of 1 to 2 V for lower-voltage devices with thinner gate oxides are common. With power MOSFETs finding increasing use in portable electronics and wireless communications where battery power is at a premium, the trend is toward lower values of $R_{dson}$ and $V_{th}$. Gate oxide quality and integrity become major issues as the gate oxide thickness is reduced to achieve lower $V_{th}$. An approximate expression for $V_{th}$ is given by:

$$V_{th} = \frac{\sqrt{4\epsilon_e K T N_A}}{\epsilon_{ox}/t_{ox}} \ln\left(\frac{N_A/n_i}{m^+}\right) + \frac{2K T}{q} \ln\left(\frac{N_A/n_i}{m^+}\right)$$  \hspace{1cm} (1.5)$$

where $\epsilon_{ox}$ and $t_{ox}$ are oxide permittivity and thickness and the other parameters are defined in Eq. (1.1).

Processing methods used and their influence on the chemistry of the silicon surface have pronounced effects on $V_{th}$. Fixed and mobile surface and interface charges as well as charges in the gate oxide act to change the value of $V_{th}$ from the intended value. Therefore, control of these charges in the process is necessary for obtaining consistent $V_{th}$ values in production. Also, the presence of mobile charges away from the gate oxide and oxide/silicon interface may find their way to the device surface over the lifetime of the device and cause a gradual shift in $V_{th}$. For example, sodium ions in the low-temperature oxide (LTO) or in the metallization can cause a shift in $V_{th}$ by changing the charge distribution at the interface. Accelerated life-tests are used by manufacturers to evaluate new processes and also to monitor $V_{th}$ shift in production. Monitoring and control of contamination in the clean room equipment are routinely carried out by capacitance-voltage measurements of test diodes.

In real devices, $V_{th}$ is altered by the unequal metal and semiconductor work functions. Denoting the barrier height between the metal and silicon oxide as $\phi_{ms}$, the work function difference is given by:

$$q \phi_{ms} = q \phi_B + q \chi_o - (q \chi + E_g/2 + q \psi_B)$$ \hspace{1cm} (1.6)$$

where $\psi_B$ is the potential difference between the intrinsic and Fermi levels in the semiconductor; $\chi$ and $\chi_o$ are the semiconductor and oxide electron affinities and $E_g$ is the semiconductor band-gap energy.

Taking into account this effect and also the various fixed and mobile charges that may alter the value of $V_{th}$ from that given above, the expression for $V_{th}$ becomes:

$$V_{th} = \phi_{ms} + 2 \psi_B - \left(\frac{Q_s + Q_{ss} + Q_i + Q_{FC}}{C_{ax}}\right)$$ \hspace{1cm} (1.7)$$

where

$Q_s$ = surface charge, which is a function of surface potential and determines channel conductivity
$Q_{ss}$ = interface state charge (typically $10^{10}$ to $10^{12}$ cm$^{-2}$); caused by dangling bonds at the semiconductor surface, these can charge and discharge with changes in the surface potential
$Q_i$ = charge due to mobile ions in the oxide
$Q_{FC}$ = fixed surface charge at the silicon–oxide interface

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It is worth mentioning that the success of silicon devices lies partly in the low density of these interface states which is due to the existence of native oxide in silicon as opposed to other semiconductors such as GaAs where such a native oxide does not exist and oxide layers have to be deposited with several orders of magnitude higher interface state densities.

**Diode Forward Voltage \( V_F \) or \( V_{SD} \)**

This is the guaranteed maximum forward drop of the body-drain diode at a specified value of source current. Figure 1.64 shows a typical \( I-V \) characteristic for this diode at two temperatures. \( p \)-Channel devices have higher values of \( V_F \) due to the higher contact resistance between metal and \( p \)-silicon compared with \( n \)-type silicon. Maximum values of 1.6 V for high-voltage devices (>100 V) and values of 1.0 V for low-voltage devices (<100 V) are common.

**Power Dissipation**

The maximum allowable power dissipation which will raise the die temperature to the maximum allowable when the case temperature is held at 25°C is an important parameter and is given by:

\[
P_d = \left( \frac{T_{j,max} - 25}{R_{thJC}} \right)
\]

where \( T_{j,max} \) is the maximum allowable temperature of the \( pn \) junction in the device (normally 150 or 175°C) and \( R_{thJC} \) is the junction to cause thermal impedance of the device.

**Dynamic Characteristics**

**Switching and Transient Response**

When the MOSFET is used as a switch, its basic function is to control the drain current by the gate voltage. Figure 1.65 shows the transfer characteristics and an equivalent circuit model often used for the analysis of MOSFET switching performance. For a detailed discussion of this topic see Chapter 4 in Grant and Gower (1989). The following is a summary of the important points.

The switching performance of a device is determined by the time required to establish voltage changes across capacitances and current changes in inductances. \( R_g \) is the distributed resistance of the gate and is approximately inversely proportional to active area. Values of around 20 \( \Omega \)-mm\(^2\) are common for the
product of $R_G$ and active area for polysilicon gates. $L_S$ and $L_D$ are source and drain lead inductances and are around a few tens of nH. The physical origin of the capacitances $C_{GS}$, $C_{GD}$, and $C_{DS}$ were discussed in the introduction of this chapter regarding the device schematic shown in Fig. 1.57. The typical values of input ($C_{iss}$), output ($C_{oss}$), and reverse transfer ($C_{rss}$) capacitances given in the data sheets are used by circuit designers as a starting point in determining circuit component values. The data sheet capacitances are defined in terms of the equivalent circuit capacitances as:

$$C_{iss} = C_{GS} + C_{GD}, \quad C_{DS} \text{ shorted}$$
$$C_{rss} = C_{GD}$$
$$C_{oss} = C_{DS} + C_{GD}$$

The gate-to-drain capacitance $C_{GD}$ is a nonlinear function of voltage and is the most important parameter since it provides a feedback loop between the output and the input of the circuit. $C_{GD}$ is also called the
Miller capacitance since it causes the total dynamic input capacitance to become greater than the sum of the static capacitances.

Figure 1.66 shows a typical switching time test circuit. Also shown are the components of the rise and fall times with reference to the $V_{GS}$ and $V_{DS}$ waveforms. Turn-on delay, $t_{d(on)}$, is the time taken to charge the input capacitance of the device before drain current conduction can start. Similarly, turn-off delay $t_{d(off)}$ is the time taken to discharge the capacitance after the gate is switched off.

**Gate Charge**

Although input capacitance values are useful, they do not provide accurate results when comparing the switching performances of two devices from different manufacturers. Effects of device size and transconductance make such comparisons more difficult. A more useful parameter from the circuit design point of view is the gate charge rather than capacitance. Most manufacturers include both parameters on their data sheets. Figure 1.67 shows a typical gate charge waveform and the test circuit. When the gate is connected to the supply voltage, $V_{GS}$ starts to increase until it reaches $V_{th}$ at which point the drain current starts to flow and the $C_{GS}$ starts to charge. During the period $t_1$ to $t_2$, $C_{GS}$ continues to charge, the gate voltage continues to rise and the drain current rises proportionally. At time $t_2$, $C_{GS}$ is completely charged and the drain current reaches the predetermined current $I_D$ and stays constant while the drain voltage starts to fall. With reference to the equivalent circuit model of the MOSFET shown in Fig. 1.67, it can be seen that with $C_{GS}$ fully charged at $t_2$, $V_{GS}$ becomes constant and the drive current starts to charge the Miller capacitance $C_{GD}$. This continues until time $t_f$. Note that the charge time for the Miller capacitance is larger than that for the gate to source capacitance $C_{GS}$ due to the rapidly changing drain voltage between $t_2$ and $t_f$ (current = $C \frac{dV}{dt}$). Once both of the capacitances $C_{GS}$ and $C_{GD}$ are fully charged, the gate voltage...
VGS starts increasing again until it reaches the supply voltage at time t4. The gate charge (QGS + QGD) corresponding to time t3 is the bare minimum charge required to switch the device on. Good circuit design practice dictates the use of a higher gate voltage than the bare minimum required for switching and therefore the gate charge used in the calculations is QG corresponding to t4.

The advantage of using gate charge is that the designer can easily calculate the amount of current required from the drive circuit to switch the device on in a desired length of time; since Q = CV and I = C dV/dt then Q = time × current. For example, a device with a gate charge of 20 nC can be turned on in 20 µs if a current of 1 mA is supplied to the gate or it can turn on in 20 ns if the gate current is increased to 1 A. These simple calculations would not have been possible with input capacitance values.

**dV/dt Capability**

This is also called the peak diode recovery and is defined as the maximum rate of rise of drain-source voltage allowed. If this rate is exceeded then the voltage across the gate-source terminals may become higher than the threshold voltage of the device, forcing the device into the current conduction mode and

![Diagram of gate charge test circuit and resulting waveforms.](image)
under certain conditions a catastrophic failure may occur. There are two possible mechanisms by which a \( \frac{dV}{dt} \) induced turn-on may take place. Figure 1.68 shows the equivalent circuit model of a power MOSFET, including the parasitic BJT. The first mechanism of \( \frac{dV}{dt} \) induced turn-on becomes active through the feedback action of the gate-drain capacitance \( C_{GD} \). When a voltage ramp appears across the drain and source terminals of the device, a current \( I_1 \) flows through the gate resistance \( R_G \) by means of the gate-drain capacitance \( C_{GD} \). \( R_G \) is the total gate resistance in the circuit and the voltage drop across it is given by:

\[
V_{GS} = I_1 R_G = R_G C_{GD} \left( \frac{dV}{dt} \right)
\]

When the gate voltage \( V_{GS} \) exceeds the threshold voltage of the device \( V_{th} \), the device is forced into conduction. The \( \frac{dV}{dt} \) capability for this mechanism is thus set by:

\[
\left( \frac{dV}{dt} \right) = \frac{V_{th}}{R_G C_{GD}}
\]

It is clear that low \( V_{th} \) devices are more prone to \( \frac{dV}{dt} \) turn-on. The negative temperature coefficient of \( V_{th} \) is of special importance in applications where high-temperature environments are present. Also, gate circuit impedance has to be chosen carefully in order to avoid this effect. \( C_{GD} \) is an internal device parameter and is determined by the overlap area between poly gate and silicon and gate oxide thickness. Higher gate oxide thicknesses reduce \( C_{GD} \) and also increase \( V_{th} \), both advantageous to \( \frac{dV}{dt} \) rating, as long as the higher \( V_{th} \) is acceptable in the application.

The second mechanism for the \( \frac{dV}{dt} \) turn-on in MOSFETs is through the parasitic BJT as shown in Fig. 1.69. The capacitance associated with the depletion region of the body diode extending into the drift region is denoted as \( C_{DB} \) and appears between the base of the BJT and the drain of the MOSFET. This capacitance gives rise to a current \( I_2 \) which flows through the base resistance \( R_B \) when a voltage ramp appears across the drain-source terminals. With analogy to the first mechanism, the \( \frac{dV}{dt} \) capability of this mechanism is given by:

\[
\left( \frac{dV}{dt} \right) = \frac{V_{BE}}{R_B C_{DB}}
\]
If the voltage that develops across $R_B$ is greater than about 0.7 V, then the base–emitter junction is forward-biased and the parasitic BJT is turned on. Under the conditions of high $dV/dt$ and large values of $R_B$, the breakdown voltage of the MOSFET will be limited to that of the open-base breakdown voltage of the BJT. If the applied drain voltage is greater than the open-base breakdown voltage, then the MOSFET will enter avalanche and may be destroyed if the current is not limited externally.

Increasing $dV/dt$ capability therefore requires reducing the base resistance $R_B$ by increasing the body region doping and reducing the distance the current $I_b$ has to flow laterally before it is collected by the source metallization. As in the first mode, the BJT related $dV/dt$ capability becomes worse at higher temperatures since $R_B$ increases and $V_{BE}$ decreases with increasing temperature.

**Applications**

The following are two of the major markets where power MOSFETs are finding increasing applications as either logic-controlled or analog switches.

**Portable Electronics and Wireless Communication**

With the recent advances in the portable electronic products, low $R_{ds(on)}$, logic level surface mount power MOSFET are experiencing explosive demand. A portable computer, for example, uses power MOSFETs in the AC-DC converters, the DC-DC converters and voltage regulators, load management switches, battery charger circuitry, and reverse battery protection. Required features of MOSFETs in these applications are small size, low power dissipation, and low on-resistance for extended battery life. Reduction of both conduction and switching losses are important considerations in the design of MOSFETs aimed at this market.

**Automotive**

Mechanical contact breakers have mostly been replaced by semiconductor devices in ignition circuits in modern cars. A suitable semiconductor device must be capable of blocking high voltages in a severe environment where line voltage surges are common due to the opening and closing of switches and the connection and disconnection of inductive loads during maintenance and loose connections. Bipolar transistors with their susceptibility to secondary breakdown are not suited whereas power MOSFETs with avalanche capability are ideally suited. Voltage transients are clamped by the avalanching of the MOSFET without the need to use any external protection circuits.

![Physical origin of the parasitic BJT components that may cause $dV/dt$-induced turn-on in power MOSFET.](image-url)
In 12-V battery vehicles the most commonly used MOSFETs are rated at 50 or 60 V breakdown voltages. The significant guard-banding is necessary in order to avoid device failure due to the alternator producing high voltages after shedding a heavy load.

The other features of power MOSFETs which make them suitable for the automotive applications are high $dV/dt$ ratings, high-temperature performance, ruggedness and high reliability. Logic level, surface mount devices with low $R_{ds(on)}$ have recently found application in this field. The smaller footprint of surface mounts offers space savings and the lower $R_{ds(on)}$ does away with the need to parallel devices to reduce on-resistance. This in turn translates into fewer device counts and heat-sinks which lowers the overall cost.

In addition to ignition control, power MOSFETs are used in anti-lock brake (ABS) systems, electronic power steering (EPS) systems, air bags, electronic suspension, and numerous motor control applications such as power windows, power seats, radiator fan, wipers, fuel pump, etc.

References

1.7 General Power Semiconductor Switch Requirements

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A power semiconductor switch is a component that can either conduct a current when it is commanded ON or block a voltage when it is commanded OFF through a control. This change of conductivity is made possible in a semiconductor by specially arranged device structures that control the carrier transportation. The time that it takes to change the conductivity is also reduced to the microsecond level compared with the millisecond level of a mechanical switch. By employing this kind of switch, a properly designed electrical system can control the flow of electric energy, shaping the electricity into desired forms.

Parameters describing the performance of a power conversion system include reliability, efficiency, size, and cost. The power switch plays an important role in determining these system-level performances [1]. To facilitate the analysis, a simple buck converter shown in Fig. 1.70a (buck converter) and 1.70b (its switching waveforms) is used as an example. There are two switches SW and $D_F$ in the circuit. The purpose of this circuit is to deliver energy from a power source with a higher voltage $V_{CC}$ to the load with a lower voltage $V_O$ requirement. When the power switch SW is on, the energy is delivered from the source $V_{CC}$ through switch SW, inductor $L$ to the load. When the output voltage is high enough, this energy link will be shut down by turning off SW. Energies stored in $L$ and $C_O$ will maintain the load voltage. The typical circuit waveforms are depicted in Figs. 1.70a and b its switching waveforms. The circuit has four different operating modes: (1) ($t_0$–$t_1$) SW off and $D_F$ on; (2) ($t_1$–$t_3$) SW turn-on and $D_F$ turn-off; (3) ($t_3$–$t_4$) SW on and $D_F$ off; (4) ($t_4$–$t_6$) SW turn-off and $D_F$ turn-on.

Generally, the following parameters are important for a semiconductor switch designed for power conversion applications:

1. Maximum current carrying capability
2. Maximum voltage blocking capability
3. Forward voltage drop during ON and its temperature dependency
4. Leakage current during OFF
5. Thermal capability
6. Switching transition times during both turn-on and turn-off
7. Capability to stand $dV/dt$ when the switch is OFF or during turn-off
8. Capability to stand $dl/dt$ when the switch is ON or during turn-on
9. Controllable $dl/dt$ or $dV/dt$ capability during switching transition
10. Ability to withstand both high current and voltage simultaneously
11. Switching losses
12. Control power requirement and control circuit complexity

The above items can be further divided into three categories: static, dynamic, and control parameters. Items 1 to 5 relate to the static performance of a switch. Both current and voltage ratings describe the power handling capability of a switch. For a certain application, devices with higher current and voltage ratings are more robust to transient overcurrent and voltage due to switching transitions or circuit faults, increasing the system level reliability. For the buck converter, the nominal current of SW when it is on
is equal to the current of the output inductor. However, SW will experience higher peak current during the turn-on period between \( t_2 \) and \( t_3 \) due to diode \( D_F \) reverse recovery. When the load \( R_L \) is shorted or \( D_F \) is fail shorted, SW will observe a much higher fault current.

Lower forward voltage drop and leakage current lead to a lower power loss, which is good from the energy efficiency and the thermal management point of view. Between \( t_2 \) and \( t_1 \), the device can turn off safely, is referred to as the reverse-biased safe operation area (RBSOA) \([4]\) of the device. Obviously, the RBSOA of a device should be larger than all its possible turn-off losses are approximately proportional to the switching times. Item 7 describes the external \( dV/dt \) immunity of the device. In a system, the switch is generally exposed to a complex electromagnetic environment. However, the state and the operation of the switch should only be controlled by its control command instead of the environment. When the switch is in the OFF state or during turn-off operation, the switch should stay OFF or continue its turn-off process no matter what the external \( dV/dt \) across its anode and cathode (or collector/emitter) is. Similarly, there is a \( dI/dt \) requirement when the switch is ON or during the turn-on transition. Devices with a large cell size such as the gate turn-on (GTO) thyristor have lower \( dI/dt \) limitations because of the longer time required for uniform current distribution.

While a good switch should be able to withstand severe dynamic voltage and current changes, it should also be able to provide the system with an acceptable electromagnetic noise. This requires the controllable \( dI/dt \) and \( dV/dt \) capabilities from the switch \([2]\). A typical turn-on operation of a switch in a power conversion system is associated with a turn-off process of another switch (or diode). The \( dI/dt \) is generally determined by the turn-on switch and shared by the turn-off switch, which may not be able to withstand the high \( dI/dt \). For example, a diode has a turn-off problem and high turn-off \( dI/dt \) may overstress it. In the buck converter, the turn-off of the diode \( D_f \) is accompanied with the turn-on of SW starting from \( t_1 \). The falling \( dI/dt \) of the \( D_f \) is equal to that of rising \( dI/dt \) of the SW. After \( t_2 \), \( D_f \) enters its reverse recovery process, experiencing its highest instant power before its current finally goes to zero. To protect these associated devices effectively, the maximum turn-on \( dI/dt \) should be limited. Similarly, a typical turn-off operation of a switch in a power conversion circuit is associated with a turn-on process of another switch (or diode). The \( dV/dt \) is generally determined by the turn-off switch and shared by the turn-on switch, which may not be able to withstand the high \( dV/dt \). The maximum \( dV/dt \) of the active switch should be limited to protect the associated switches. Both \( dV/dt \) and \( dI/dt \) controls normally require a device to possess a forward-biased safe operation area (FBSOA) \([3]\). The FBSOA defines a maximum \( V-I \) region in which the device can be commanded to operate with simultaneous high voltage and current. The device current can be controlled through its gate (or base) and the length of the operation is only limited by its thermal limitation. Devices with FBSOA normally have an active region in which the device current is determined by the control signal level, as is shown in Fig. 1.71. It should be noted, however, that \( dI/dt \) control in practice means slowing down the transient process and increasing the turn-on loss.

During a typical inductive turn-off process, the voltage of a switch will rise and its current will decrease. During the transition, the device observes both high voltage and high current simultaneously. Figure 1.72 depicts the typical voltage–current trajectory of an inductive turn-off process as is the case in the buck circuit shown in Figs. 1.70a and b, between \( t_1 \) and \( t_3 \) in time domain. The current of the device stays constant while its voltage rises. Its current begins to decrease once its voltage reaches its nominal value. The voltage spike is caused by the \( dI/dt \) and stray inductance in the current commutation loop. On the \( V-I \) plane of the device, the curve that defines the maximum voltage and current boundary within which the device can turn off safely, is referred to as the reverse-biased safe operation area (RBSOA) \([4]\) of the device. Obviously, the RBSOA of a device should be larger than all its possible turn-off \( V-I \) trajectories. Devices without a large enough RBSOA need an external circuit (such as an auxiliary soft-switching circuit.
or a \( \frac{dV}{dt} \) snubber) to shape their turn-off \( I-V \) trajectories to a smaller one to ensure safe turn-off operation. Devices with turn-off snubbers can therefore survive with a much smaller RBDSOA. However, a \( \frac{dV}{dt} \) snubber increases the component count of the system, hence the system's size and cost. The turn-off operation conducted without the help of a snubber is called snubberless turn-off or hard turn-off, whereas a process with the help of a snubber is called snubbed turn-off.

During the turn-on transition, a switch will also observe both high voltage and high current simultaneously. Figure 1.73 depicts the typical voltage–current trajectory of an inductive turn-on process as is the case in the buck circuit shown in Fig. 1.70 between \( t_1 \) and \( t_3 \) in time domain. The voltage of the device stays constant while its current increases until it hits the nominal current level of the device. The current overshoot is due to the reverse recovery of an associated diode (or a switch). A device without a large enough FBDSOA needs an external snubber circuit to help its \( I-V \) trajectory, as is shown in Fig. 1.73. The stress on the device can be significantly reduced with the turn-on snubber. However, a turn-on snubber circuit also increases the component count, size, and cost of a system.
Item 10 defines the capability of a switch to withstand high instant power. However, this capability during turn-on and turn-off will be different for a semiconductor device because of the difference in free carrier distribution. RBSOA is mostly used to describe the turn-off capability of a device, while FBSOA is used to measure its turn-on capability. FBSOA, as implied by its name, is also used to measure the ability of a device to withstand high voltage and high current under DC and short-circuit conditions.

A load short circuit is a threat to the device that is ON or is turning on in a typical circuit. A temporary load short can introduce an extremely high current that generates high instant power dissipation, leading to the failure of the switch. To effectively protect the switch under a short-circuit condition, the ability to limit its maximum current at a given DC voltage is required. In this case, the peak instant power is \( V_{CC}I_{\text{LIM}} \), whereas for a device without this ability it is \( V_{CC}/r \), where \( V_{CC} \) is the DC voltage, \( I_{\text{LIM}} \) is the maximum current limitation of the device, and \( r \) is the effective resistance of a device while it is ON. Since \( r \) is normally low in a practical device, the instant power of a device under a load short circuit without the maximum current limitation is much higher. Figure 1.74 shows the \( I-V \) characteristics during the ON state for devices with or without the self-current limitation capability.
The ability of a switch to limit its maximum current regardless of the voltage applied is an effective method to limit its instant power. A device with FBSOA capability normally has self-current limiting capability and, hence, can survive a short-circuit fault for a short time as determined by its thermal limitation [5].

References
2. R. Chokhawala et al., Gate drive considerations for IGBT modules, presented at IAS '92, 1992, 1186–1195.

1.8 Gate Turn-Off Thyristors

Alex Q. Huang

The first power semiconductor switch that was put in use was the silicon controllable rectifier (SCR) [1] invented in 1950s. The SCR is a latch-up device with only two stable states: ON and OFF. It does not have FBSOA. It can be switched from OFF to ON by issuing a command in the form of a small gate-triggering current. This will initiate a positive-feedback process that will eventually turn the device on. The SCR has a good trade-off between its forward voltage drop and blocking voltage because of the strong conductivity modulation provided by the injections of both electrons and holes. Moreover, the structure of an SCR is very simple from a manufacturing point of view because its gate can be placed at one small region. The size of a single SCR can therefore be easily expanded to increase the current capability of the device without too many processing problems. There are 8.0 kA/10.0 kV SCRs commercially available that use a 6-in. silicon wafer for current conduction. However, SCRs cannot be turned off through their gate controls.

Because of the limitation of the turn-off controllability of the SCR, the gate turn-off (GTO) thyristor [2] was subsequently developed. As its name denotes, a GTO is a device that can be turned off through its gate control. Its basic structure is very similar to that of an SCR. However, many gate fingers are placed in the GTO surrounding its cathode. During a turn-off operation, the latch-up mechanism can be broken through the gate control. A GTO is thus a device with full gate control and similar high current–voltage rating of an SCR. To date, the GTO has the highest power rating and the best trade-off between the blocking voltage and the conduction loss of any fully controllable switch. However, the dynamic performance of GTOs is poor. A GTO is slow in both turn-on and turn-off. It lacks FBSOA and has poor RBSOA so it requires snubbers to control \( \frac{dV}{dt} \) during the turn-off transition and \( \frac{dI}{dt} \) during turn-on transition.

The GTO thyristor was one of the very first power semiconductor switches with full gate control. It has served many power applications ranging from low power (below 100 W) in its early years to high power up to hundreds of megawatts. A state-of-the-art GTO can be fabricated on a silicon wafer as big as 6 in. and can be rated up to 6.0 kA and 6.0 kV [3]. This rating is much higher than the ratings of any other fully controllable devices.

The GTO static parameters are excellent: low conduction loss due to its double-sided minority carrier injection, high blocking voltage, and low cost due to its fabrication on a large single wafer. However, its dynamic performance is poor. The requirements of a \( \frac{dV}{dt} \) snubber during turn-off operation, a \( \frac{dI}{dt} \)
snubber during turn-on operation, and minimum on and off times make the GTO difficult to use. To improve the dynamic performance of the GTO while keeping its good static performance, a better understanding of the mechanism of the GTO is necessary. In this section, the basic operating principle of the GTO, its advantages and disadvantages, and the mechanism that determines its performance are summarized and discussed. A new gate-driving concept, namely, unity-gain turn-off, is then introduced. The advantages of this special driving method are analyzed and discussed. Finally, all known approaches that make use of this special driving technique are summarized.

**GTO Forward Conduction**

Figure 1.75a illustrates the cell structure and the doping profile of a typical high power GTO. Figure 1.75b shows the two-transistor GTO model; and Fig. 1.75c is a photograph of a 4-in. GTO along with its gate lead. The structure is a three-terminal, four-layer \( pnpn \) structure with a lightly doped \( n^- \) voltage-blocking layer in the center [4]. The electrode on the external \( p^+ \) layer is called the anode where the current normally flows into the device. The electrode on the external \( n^- \) layer is called the cathode from where the current normally flows out. The electrode on the internal \( p \) layer (\( p \)-base) is called the gate, which is used for control.

The operating principle of a GTO can be understood through its equivalent circuit model shown in Fig. 1.75b. The \( pnp \) transistor represents the top three layers of the GTO, whereas the \( npn \) transistor

![Figure 1.75](image-url)
represents the bottom three layers of the GTO. Since the $n^-$ layer serves as the base of the $pnp$ and the collector of the $npn$, and the internal $p$ layer serves as the base of the $npn$ and the collector of the $pnp$, the two transistors are cross-coupled. This structure has two stable states: ON and OFF, which are determined by its gate control. When a current is injected into the GTO from its gate to its cathode, the $npn$ structure is turned on and its collector current flows from the anode of the GTO through $J_1$ junction. Since $J_1$ is the emitter junction of the $pnp$ structure, the collector current of the $pnp$ is then the base current of the $npn$. The two transistors therefore provide base currents to each other, forming a positive feedback among them until they reach a self-sustaining state commonly known as latch-up or latched. Under the latched condition, high-level minority carrier injections are available from the anode to the cathode, with all three $pn$ junctions forward-biased. A high conductivity therefore exists from anode to cathode, allowing high current to flow from the anode to the cathode. Figure 1.76 illustrates this turn-on process.

At the silicon level, the turn-on of junction $J_3$ results in the injection of electrons into the $p$-base region. These electrons diffuse across the $p$-base and are mostly collected by the reverse biased junction $J_2$. To maintain the continuity of the current, junction $J_1$ will supply a current by injecting holes into the $n^-$ region. Part of these holes will diffuse across the $n^-$ region and are collected by junction $J_2$, resulting in more electron injection from junction $J_3$. When both transistors operate at sufficient current gain, a positive feedback mechanism is sufficient to result in latch-up.

Let the common base current gain of the $pnp$ and $npn$ be $\alpha_{pnp}$ and $\alpha_{npn}$, respectively. Normally, $\alpha_{pnp}$ is lower than $\alpha_{npn}$ since the $pnp$ is a wide-base structure. The current flow inside a GTO is illustrated in Fig. 1.77. At junction $J_2$, the current due to cathode side injection is $\alpha_{npn}I_K$; the current due to anode side...
injection is $\alpha_{pnp} I_A$, and the leakage current is $I_L$. According to Kirchhoff’s law,

$$ I_A = \alpha_{pnp} I_A + \alpha_{npn} I_K + I_L $$

and

$$ I_A = I_K - I_G $$

Combining these equations,

$$ I_A = (\alpha_{pnp} I_G + I_L)/(1 - \alpha_{pnp} - \alpha_{npn}) $$

This equation shows that the thyristor structure can sustain its anode current by itself once the sum of the common base current gain ($\alpha_{pnp} + \alpha_{npn}$) of both transistors is approaching unity. For a GTO, $\alpha_{npn}$ is designed low and is normally depending on $I_G$ to ensure its gate turn-off capability. This will be discussed later. With this self-sustaining capability, the gate of a GTO does not need to supply a lot of current and does not need to be very close to its cathode as is necessary in a bipolar junction transistor (BJT) design. The dimension of a typical GTO cell shown in Fig. 1.75 is 100 to 150 $\mu$m wide. This is very large compared with the micron and/or even submicron process used for modern MOSFETs and insulated gate bipolar transistors (IGBTs). The large cell size design is cost-effective and makes it possible to fabricate large single-die devices to boost their current capability. A state-of-the-art GTO die is as large as 6-in. in diameter with a turn-off current capability of up to 6.0 kA [3]. Figure 1.75c shows a large GTO fabricated by ABB. The GTO shown is fabricated on a 4-in. silicon wafer consisting of thousands of cells like the one shown in Fig. 1.75 and packaged in a so-called press-pack or hockey-puck package.

The large cell structure in the GTO introduces a current spreading problem during the turn-on transition of a GTO. When a gate current is injected, the turn-on occurs first in the vicinity of the gate contact. The conduction area then spreads across the rest of the cathode area. This can be characterized by a propagation velocity called the spreading velocity [5]. Experimental measurements [6] have shown a typical spreading velocity of 5000 cm/s. This velocity also depends on the GTO design parameters, the gate turn-on injection current, and its $\frac{dI}{dt}$.

Because of this spreading velocity, it takes time for the whole GTO cell to turn on. To avoid overstressing the part of the cell that is turned on first, the increasing rate of the anode current should be limited. This sets the maximum turn-on $\frac{dI}{dt}$ limitation for a GTO.

The major advantages of the GTO are its low forward voltage drop and high-voltage blocking capability. These can be understood as the major benefits of its double-side minority carrier injection mechanism. For high-voltage GTO, a thick and lightly doped $n$-base is needed (see Fig. 1.75). The forward voltage drop in this case is mainly determined by the resistive voltage drop in the voltage-blocking region where minority carriers play an important role.

Figure 1.78a shows the minority carrier distribution in the $n^-$ region of a GTO and Fig. 1.78b shows the case of an IGBT (see Section 1.9). For the same blocking voltage design, their $n^-$ regions should have similar thickness and doping. Since there is only one transistor in the IGBT structure, minority carriers can only be injected from one side; therefore, the conductivity modulation in the $n^-$ region is weaker than that of the GTO. In the GTO, since there are two transistors, minority carriers can be injected from both ends, making a more uniform plasma distribution in the whole area. For a 4.5-kV state-of-the-art GTO, its forward voltage drop at a current density of 50 A/cm$^2$ can be as low as 2.0 V [7] if a constant gate current injection presents. Figure 1.79 shows the on-state characteristics of a state-of-the-art GTO manufactured by ABB [7]. The forward voltage drop at 2000 A is only about 1.5 V for this 4.5-kV GTO. This result is typical of a low conduction loss GTO.
GTO Turn-Off and Forward Blocking

If the GTO gate is pulling out current from the GTO, the current injection into the \( npn \) base will be reduced. Once this is reduced below a certain level, the collector current of the \( npn \), and hence the base current of the \( pnp \), will also decrease, leading to the reduced \( pnp \) collector current. This will further reduce the base current of the \( npn \) since it is the difference between the collector current of the \( pnp \) and the gate pullout current. This positive-feedback process will eventually turn off the GTO.

Figure 1.80 shows the current flow inside the GTO when its gate is pulling out current to turn off the device. The base drive current required to maintain current conduction in the \( npn \) transistor is \( (1 - \alpha_{npn})I_K \). The base drive current available to the \( npn \) transistor in this case is \( \alpha_{pnp}I_A - I_G \). Thus, the condition to turn off the GTO through the gate control is given by:

\[
\alpha_{pnp}I_A - I_G < (1 - \alpha_{npn})I_K \tag{1.15}
\]

Since

\[
I_K = I_A - I_G \tag{1.16}
\]

the condition to turn off the GTO is

\[
I_G > \frac{(\alpha_{pnp} + \alpha_{npn} - 1)}{\alpha_{npn}} I_A \tag{1.17}
\]
The ratio of the anode current to the gate current at which level a GTO is turned off is defined as the turn-off gain. From Eq. (1.17), the maximum turn-off gain \[4\] can be expressed as:

\[
\beta_m \equiv \frac{I_A}{I_G} = \frac{\alpha_{npn}}{\alpha_{pnp} + \alpha_{npn} - 1}
\] (1.18)

A large turn-off gain is normally desirable to reduce the current requirements of the gate driver. A lower \((\alpha_{pnp} + \alpha_{npn})\) value is necessary to ensure a reasonable turn-off gain. It is also important to point out that \(\alpha_{npn}\) in Eq. 1.18 is not a constant; normally it decreases when gate current \(I_G\) increases.

When a GTO is OFF, its junction \(J_3\) is reverse-biased and can support a high voltage applied between its anode and cathode, as shown in Fig. 1.81a. If the junction \(J_3\) is reverse-biased or shorted by the gate

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**FIGURE 1.79** On-state characteristics of 5SGT 40L4502, a 4-kA, 4.5-kV GTO from ABB.

**FIGURE 1.80** Current flow inside the GTO when its gate is pulling out current.
driver, the maximum forward blocking voltage $BV_{AK}$ of the GTO is determined by the avalanche breakdown capability of the $pnp$ transistor under the open-base condition [8]. This voltage can be expressed as:

$$BV_{AK} = (1 - \alpha_{pnp})^{1/n}BV_{J2}$$  \hspace{1cm} (1.19)\)

where $\alpha_{pnp}$ is the common base current gain of the $pnp$ structure at low current levels; $n$ is an empirical constant, and $BV_{J2}$ is the avalanche breakdown voltage of the $pn$-junction $J_2$. Since this $pnp$ has a wide base structure, its common base current gain $\alpha_{pnp}$ is low compared with a normal bipolar transistor. Thus, the forward voltage blocking capability $BV_{AK}$ of a GTO is very close to the breakdown voltage of junction $J_2$.

A GTO can also block a reverse voltage by its junction $J_1$, as shown in Fig. 1.81b. When the junction $J_1$ is gated off, the reverse voltage blocking capability is similarly determined by the avalanche breakdown of the $pnp$ structure under the open-base condition. A GTO with both forward and reverse blocking capability is called symmetric blocking GTO. Most GTOs manufactured today, however, are asymmetric GTOs because the reverse blocking capability is not utilized ($J_1$ junction not designed to support high reverse voltage) or cannot be utilized because of other design requirements, such as the need to introduce anode-short at junction $J_1$ to speed the turn-off.
Practical GTO Turn-Off Operation

The turn-off capability of a GTO is limited dominantly by a non-uniform current distribution (also called current filamentation) problem during turn-off transient. This causes current to concentrate to a few GTO cells and destroy the device with the high power stress. Furthermore, the current filamentation is believed to be initiated by the dynamic avalanche (see next section) in an inhomogeneous, large-area GTO.

A GTO normally requires a $dV/dt$ snubber circuit to conduct actual turn-off operation under high voltage and high current condition. This is because a large current GTO turn-off will fail without such a $dV/dt$ snubber as a result of its small RBSOA. This small RBSOA is caused by a non-uniform current distribution or current filamentation problem in the GTO.

Figure 1.82 shows a practical setup in which a typical $dV/dt$ snubber formed by $D_s$, $R_s$, and $C_s$ is used, and Fig. 1.83 shows a typical GTO turn-off characteristic under snubbed condition. Before $t_0$, the GTO is ON, so a current is built up in the load inductor $L_L$ and the device under test (DUT). The anode current $I_A$
is approximately equal to the cathode current $I_K$ because the gate current $I_G$ is negligible. Starting from time $t_0$, a negative voltage $V_{OFF}$ is applied to the gate of the GTO. The gate current $I_G$ then decreases linearly at a rate determined by the applied negative turn-off gate voltage $V_{OFF}$ and the gate lead stray inductance $L_G$. At $t_1$, the device could not maintain the latch any longer so the anode current begins to decay. The current from the load inductor is diverted to the $dV/dt$ snubber path. At $t_2$, when the anode current observes its maximum $dI/dt$, the anode voltage shows a spike due to the stray inductance $L_S$ in the $dV/dt$ snubber path. At $t_3$, the anode current enters its tail stage. At $t_4$, the anode voltage reaches the DC link voltage so the freewheeling diode $D_F$ will be conducting. The energy in the stray inductance in the loop of power supply, freewheeling diode, and the $dV/dt$ snubber is released to the snubber capacitor, causing another voltage peak. The anode voltage dip between $t_4$ and $t_5$ is due to the reverse recovery of the $dV/dt$ snubber diode $D_S$. The turn-off trajectory of a GTO with a $dV/dt$ snubber is significantly reduced, as shown in Fig. 1.72 (see Section 1.7 on General Power Semiconductor Switch Requirements).

**Dynamic Avalanche**

Under a high electric field, an avalanche process occurs within the silicon. The static critical electric field is a function of the doping profile. The lower the doping, the lower the critical avalanche electric field. The static avalanche voltage of a single side abrupt $pn$-junction is determined by both the critical electric field and the depletion region width.

While the reverse-biased junction conducts high current, as is the case of a GTO turn-off with or without a $dV/dt$ snubber, the avalanche voltage decreases significantly because of the existence of carriers in the depletion region. This process is called dynamic avalanche [9]. Figure 1.84 shows the cross section of a $pnp$ transistor under both current and voltage stress. A GTO turn-off with a $dV/dt$ snubber enters the $pnp$ conduction mode between $t_2$ and $t_3$, as shown in Fig. 1.82. Assuming carriers in the depletion region are moving at their saturation speed, then both the anode current density and the anode–cathode voltage can be expressed as:

\[
J_A = q p v_s \quad (1.20)
\]
\[
V_{AK} = E_m W_g / 2 \quad (1.21)
\]
\[
= (\varepsilon_s E_c^2) / 2 q p = (\varepsilon_s E_c^2) / (J_A / v_s) \quad (1.22)
\]

where $p$ is hole density in the depletion region, $E_c$ is the critical electric field causing avalanche breakdown, and $v_s$ is the saturation velocity of holes. In the depletion region, holes are the only carriers. In the presence of holes in the depletion region, the charge density in the depletion region is higher compared with the case without the current, so the peak electric field is also higher at the same width of the depletion region.
At the point when dynamic avalanche happens, the power density of the device, which is the product of both the current and the voltage applied on the device, can thus be expressed as:

\[ J_A V_{AK} = \varepsilon \nu C_e E_c^2 / 2 \]  

which is about 200 to 300 kW/cm\(^2\) for silicon.

The onset of dynamic avalanche itself is not a stable condition because the generated carrier is not sufficient to maintain the current. Hence it is not a failure condition from the point of view of the physics of the device. The dynamic avalanche is, however, widely regarded as the failure mechanism of the GTO because it will initiate a non-uniform current distribution among large-wafer-size GTOs. The current crowding or current filament formed after the onset of dynamic avalanche is enough to destroy the device at one location in the form of a melted spot [10].

**Non-Uniform Turn-Off Process among GTO Cells**

For a high-power GTO, the experimentally obtained instant turn-off power it can withstand is far below the value set by the dynamic avalanche breakdown shown in Eq. (1.21). So a GTO needs help from a \(dV/dt\) snubber to shape its turn-off \(I-V\) trajectory, as is shown in Fig. 1.72, and to lower the maximum average instant power the external circuit can apply. Non-uniform current distribution or current filament [10] among GTO cells during the turn-off operation accounts for this limitation. The current filament can be formed at the beginning of the turn-off due to differences in storage times or caused by the onset of the dynamic avalanche during the turn-off when the voltage and current are both high [11].

**Current Filamentation Caused by Storage Time Difference**

The non-uniform turn-off process can be understood by considering two GTO cells in parallel, as is shown in Figs. 1.85 and 1.87. The two cells are identical except for their storage time. This storage time difference is considered unavoidable in high-current GTOs because of differences in carrier lifetime, wafer thickness, and doping. Although only two cells are shown, GTO1 can represent a group of slower cells whereas GTO2 represents a group of faster cells. The turn-off process starts from \(t_0\). Since it has a shorter storage time, GTO2 turns off earlier at \(t_1\). The current originally shared by GTO2 is now transferred to GTO1. At \(t_2\), GTO1 is turned off at twice its previous current. Turn-off failure can happen if its current at \(t_2\) exceeds the maximum turn-off capability of GTO1. This can easily be the case when the number of faster cells is much larger than the number of slower cells. This type of failure typically occurs at the very beginning of the GTO turn-off before voltage rises and is caused by a rapid formation of current filament due to storage time difference.

What makes this type of failure likely is that there is also a positive feedback mechanism that will further increase the storage time difference, as shown in Fig. 1.86. At higher current density, the common-base
current gains of both transistors in GTO1 increase. Thus, its turn-off gain becomes even lower according to Eq. (1.16), requiring more gate current for turn-off, hence increasing its storage time. Considering that the typical storage time of a high-current GTO is in the range of $20 \mu s$, there is enough time for the dangerous current filament to form.

**Current Filamentation Caused by Onset of Dynamic Avalanche**

Even if the above-discussed failure did not occur because GTO1 is beginning to turn off before the current filament density is too high, another failure mechanism can exist. At $t_2$, where both current and voltage are high, GTO1 is subject to much higher instant power stress than that of GTO2. The dynamic avalanche could then occur first at GTO1 and initiate another positive feedback that will further increase the localized current density (hence the name current filament) and enable the relatch of GTO1. Dynamic avalanche in a few cells can be viewed as an effective increase in the conductivity of those cells. If the number of slower cells is much smaller than that of faster cells, the current density in GTO1 can then become extremely high. This process can occur very quickly around $t_3$ with the area of the current filament smaller and smaller and the current density higher and higher (due to positive feedback). The excessive energy

---

**FIGURE 1.85** Current crowding among two GTO cells as a result of their storage time difference.

**FIGURE 1.86** Positive feedback mechanism enhances the storage time difference and pushes the current filament into the slowest cell.
dissipated on the stressed cells can cause permanent failure because the temperature can be very high. After the device failure, a GTO device loses its blocking capability and behaves resistively.

It can therefore be concluded that the combination of storage time differences and the onset of possible localized dynamic avalanche makes the turn-off capability of a GTO small. Practical RBSOAs of high-power GTOs are below the 50 kW/cm² power constant line. This low limitation mandates the use of a \( \frac{dV}{dt} \) snubber. Even with a \( \frac{dV}{dt} \) snubber, GTO failure can still occur if the instant power is too high at \( t_2 \) and exceeds the RBSOA limit of the GTO at that time instance. The voltage spike at \( t_2 \) can be reduced by minimizing the stray inductance of the \( \frac{dV}{dt} \) snubber. The size of the snubber (\( C_s \) value) is typically between 3 to 6 \( \mu \)F. The disadvantages of using a \( \frac{dV}{dt} \) snubber are the increased count and size of the components, its high-energy loss, and its increased thermal management requirement to cool resistor \( R_s \).

The concerns of non-uniform current distribution also mandate a minimum on-time rating for GTOs to ensure that conduction current is uniformly distributed in the ON state before a turn-off can be performed. Minimum off-time is also a commonly used rating for the GTO to guarantee the tail current of the GTO is completely gone and the GTO cells are all in the OFF state.

**Summary**

Advantages of the GTO include:

1. High current—voltage capability
2. Low conduction loss
3. Low cost

Disadvantages

1. Non-uniform turn-off—poor RBSOA and \( \frac{dV}{dt} \) snubber required
2. Non-uniform turn-on—\( \frac{dl}{dt} \) snubber required
3. Current control—high gating power
4. Long switching time—long storage time, minimum on-time and off-time requirements
5. No current limitation capability (FBSOA)
1.9 Insulated Gate Bipolar Transistors

Alex Q. Huang

When the development of power MOSFETs encountered difficulty in increasing their current-handling capability, the idea of a MOS-controlled bipolar device was developed to overcome the problem. This effort led to today’s insulated gate bipolar transistor (IGBT) [1]. The IGBT fundamentally changes the BJT current control into voltage control while maintaining the advantages of the BJT. In addition, the use of a wide-base $pnp$ transistor in the IGBT structure results in a much improved conductivity modulation effect than a conventional BJT, pushing the voltage rating of the IGBT toward the level of GTOs. The internal $pnp$ structure also does not have the second breakdown problem as a conventional $npn$ structure because the high voltage is supported by the base region of the $pnp$ transistor instead of by the collector region as is the case for a conventional $npn$ transistor. IGBTs also have excellent RBSOA and FRSOA. Having undergone several years’ development, IGBTs have become the best device for applications in the range of 600 to 3000 V.

Although there are a number of other devices that have been developed or are being developed, the workhorse power semiconductor devices today are SCRs, GTOs, MOSFETs, and IGBTs. Each of these devices dominates a specialized power arena. The MOSFET has excellent dynamic and static performance. It dominates low voltage applications below 600 V. The IGBT is slower than the MOSFET but has better forward voltage drop above 600 V. It dominates applications from 600 to 3000 V. At an even higher voltage level, the GTO becomes the dominant device with better current-carrying capability but much slower dynamic response. Without turn-off capability, the SCR has an even better current conduction capability, so it is suitable for even higher power AC applications where gate-controlled turn-off capability is not necessary.

For a typical application, the switching frequency is an important index in determining system performance. Generally, the higher the switching frequency, the better the dynamic performance of the system, the smaller the size of the system due to reduced passive components, and the lower the cost of the system due to savings on passive components. The practical switching frequency of an application system is a trade-off of many issues including maximum device switching frequency, maximum magnetic switching frequency, switching losses of the power switches, overall system efficiency, etc. In the low power field where the MOSFET plays the major role, the switching frequency is normally subject to
system efficiency and/or magnetic considerations instead of device limitations. In the medium power field, where the IGBT plays the major role, the situation changes. At the lower end, the limitation of the device does not dominate since the lower-rating IGBT is normally fast enough. However, when the power rating is higher, the IGBT switching speed decreases and the switching losses increase significantly. The practical switching frequency is thus subject to the limitation of the device. When the power level moves even higher, the GTO is the only available device. Since it has several tens of microseconds switching time, significant turn-off, and \(dV/dt\) snubber loss, the GTO is traditionally the limitation of the switching frequency of the system.

The above trend shows that when the power level moves higher, power semiconductor devices limit the maximum system switching frequency, hence the performance of the system, especially at the GTO level. To meet the increasing demand for better performance in high-power systems, many efforts have been made to improve the performance of high-power semiconductor devices. Among them, one effort is to push the IGBT toward higher power ratings based on the module concept. With its good dynamic performance, high-power systems equipped with IGBTs can operate at a much higher switching frequency and have many benefits compared with a conventional GTO system. The state-of-the-art IGBT rating is currently 3.3 kV/1.2 kA [2], which is at the low end of that of the GTO.

IGBT Structure and Operation

The name insulated gate bipolar transistor stems from its operation based on an internal interaction between an insulated-gate FET (IGFET) and a bipolar transistor. It has previously been called an IGT (insulated-gate transistor), an IGR (insulated-gate rectifier), a COMFET (conductivity-modulated field-effect transistor), a GEMFET (gain-enhanced MOSFET), a BiFET (bipolar FET), and an injector FET. IGBTs have been successfully used since they were first demonstrated in 1982 and are currently the most widely used power semiconductor switches with applications from several kilowatts to a few megawatts.

A cross section of the planar junction–based IGBT structure introduced in the 1980s is shown in Fig. 1.88a. The IGBT structure is similar to that of a planar power MOSFET except the difference in the substrate doping type. The fabrication of the IGBT therefore is almost the same as a power MOSFET. This has made its manufacture relatively easy immediately after conception, and its ratings have grown at a rapid pace as a result of the ability to scale up both the current and the blocking voltage ratings. Today, the largest single-chip IGBT can carry about 100 A and block more than 3000 V. Larger current IGBTs are also introduced by paralleling more IGBT chips in a single package. These IGBTs are also called IGBT modules. Figure 1.89 shows a photograph of a 1200-A, 3300-V IGBT module fabricated by Mitsubishi.

![IGBT Structure Diagram](image)

**FIGURE 1.88** (a) Cross section of the IGBT structure and (b) equivalent circuit for the IGBT.
The equivalent circuit for the IGBT, shown in Fig. 1.88b, consists of a wide-base $pnp$ bipolar transistor driven by a short-channel MOSFET. Notice the main current path for the IGBT is not through the $pnp$ transistor but through the indicated path. In the IGBT structure, when a positive bias voltage larger than the threshold voltage of the DMOS channel is applied to the gate electrode, an inversion layer is formed along the $p$-base surface of the DMOS, and the DMOS channel is turned ON. Also an accumulation layer of electrons is formed at the surface of the $n$ region below the gate. When a positive bias is applied to the collector, electrons flow from the $n^+$ emitter contact via the DMOS channel and the accumulation layer into the $n^-$ drift region. This provides the base drive current for the vertical $pnp$ transistor in the IGBT structure. Since the emitter junction ($J_1$) for this bipolar transistor is forward-biased, the $p^+$ region injects holes into the $n^-$ base region. When the positive bias on the collector terminal of the IGBT is increased, the injected hole concentration increases and reduces the resistance of the $n^-$ drift region. Consequently, the IGBT can operate at much higher current densities than the VDMOS even when it is designed to support high blocking voltages.

As long as the gate bias is sufficiently large to produce a strong inversion layer and an accumulation layer of electrons at the $n^-$ base region surface, the IGBT forward conduction characteristic resembles that of a $pin$ diode. Therefore, the IGBT can also be considered a $pin$ diode in series with a MOSFET. Electron injections are provided by the accumulation layer electrons beneath the gate and between the adjacent $p$-body regions. However, not all injected holes recombine with these electrons; instead, some of the holes are collected by the $p$-body region, which acts as the collector region of the parasitic $pnp$ transistor. IGBT design for low conduction drop requires minimizing the parasitic $pnp$ transistor current and maximizing the $pin$ current that maximizes the conductivity modulation.

However, if the DMOS channel becomes pinched off and the electron current saturates, the hole current also saturates because of the saturation of the base drive current for the $pnp$ transistor. Consequently, the device operates with current saturation in its active region with a gate-controlled output current. This current saturation characteristic is useful for applications in which the device is required to sustain a short-circuit condition.

When the gate voltage is lower than the threshold voltage of the DMOS, the inversion layer cannot sustain and the electron current via the DMOS channel is terminated. The IGBT then operates in the
forward blocking mode. A large voltage can then be supported by the reverse-biased $p$-base/$n$-drift junction ($J_2$). Figure 1.90 shows a typical output characteristic of the IGBT.

The IGBT was the first commercially successful device based upon combining the physics of MOS-gate control with bipolar current conduction. Due to the injection of a high concentration of holes from the $p^+$ substrate into the $n^-$ drift, the conductivity of the long $n^-$ region is modulated and the IGBT exhibits pin diode-like on-state characteristics with a low forward voltage drop. Thus, the IGBT exhibits excellent current-carrying characteristics with forward conduction current densities 20 times higher than that of a power MOSFET and five times greater than that of a bipolar transistor operating at a current gain of 10. Since the input signal for the IGBT is a voltage applied to the MOS-gate, the IGBT has the high input impedance of the power MOSFET and can be classified as a voltage-controlled device. However, unlike the power MOSFET, the switching speed of the IGBT is limited by the time taken to remove the stored charges in the drift region due to the injection of holes during on-state current conduction. The turn-off time for the IGBT is dictated by the conduction modulation of the drift region and the minority carrier lifetime. The frontier is specified dominantly by the current gain of the wide-base $pnp$ transistor, and the latter can be controlled by a lifetime control process, such as electron irradiation. Although the lifetime control process can be successful in reducing the turn-off time, it was found that there was a trade-off between the on-state voltage drop (conduction loss) and the turn-off time (switching loss). A shorter minority carrier lifetime makes the switching loss of the IGBT lower, but the shorter minority carrier lifetime also results in a higher conduction loss.

One of the problems encountered when operating the IGBT at high current levels has been the latch-up of the parasitic $pnpn$ thyristor structure inherent in the device structure. Latch-up of this thyristor can occur, causing losses of gate-controlled current conduction. Since the current gains of the $nnp$ and $pnp$ transistors increase with increasing temperature, the latching current decreases with increasing temperature. This effect is also aggravated by an increase in the resistance of the $p$-base with temperature due to a decrease in the mobility of holes. Many methods have been explored to suppress the latch-up of the parasitic thyristor, such as the use of a deep $p^+$ diffusion, a shallow $p^+$ diffusion, or a self-aligned sidewall diffusion of $n^+$ emitter. State-of-the-art IGBTs have basically solved this problem, and latch-up does not occur for all gate voltages applied. These IGBTs therefore exhibit close to square FBSOA.

Traditionally, IGBTs are fabricated on a lightly doped epitaxial substrate, such as the one shown in Fig. 1.88a. Because of the difficulty of growing the lightly doped epitaxial layer, the breakdown voltage of this type of IGBT is limited to below 1000 V. To benefit from such a design, an $n$ buffer layer is normally introduced between the $p^+$ substrate and the $n^-$ epitaxial layer, so that the whole $n^-$ drift region is depleted when the device is blocking the off-state voltage, and the electric field shape within the $n^-$ drift region is close to rectangular. This type of design is referred to as Punch-Through IGBT (PT IGBT), as shown in Fig. 1.91a. The PT structure allows it to support the same forward blocking voltage with about half the thickness of the $n^-$ base region of the $pnp$ transistor, resulting in a greatly improved trade-off relationship between the forward voltage drop and the turn-off time. Thus, the PT structure together with lifetime control is preferred for IGBTs with forward blocking capabilities of up to 1200 V.
For higher blocking voltages, the thickness of the drift region becomes too large for cost-effective epitaxial growth. Another type of design, the Non-Punch-Through IGBT (NPT IGBT, as shown in Fig. 1.91b), is gaining popularity. In the NPT IGBTs, devices are built on an $n^-$ wafer substrate that serves as the $n^-$ base drift region. The collector is implanted from the backside of the wafer after proper wafer thinning, and no field stopping $n$ buffer layer is applied to the NPT IGBT. In this concept, the shape of the electric field is triangular in the forward blocking state, which makes a longer $n^-$ base region necessary to achieve the same breakdown voltage as compared with the PT IGBT. However, the NPT IGBT offers some advantages over the PT IGBT. For example, the injection efficiency from the collector side can be controlled (due to the use of implanted $p^+$ region) and devices with voltage ratings as high as 4 kV can be realized. Further, by optimizing the emitter efficiency of carriers from the $p^+$ collector layer and the transport factor of carriers in the $n^-$ base, the trade-off between the forward voltage drop and the turn-off time for the NPT IGBT can be improved to become similar to that of the PT type IGBT without lifetime control.

Generally speaking, the current tail in the NPT IGBT is longer than the PT IGBT, but the NPT IGBT is more robust than the PT IGBT, particularly under a short-circuit condition. The trench gate IGBT (UMOS-gate IGBT) structure is shown in Fig. 1.91c. With the UMOS structure in place of the DMOS gate structure in the IGBT, the channel density is greatly increased and the JFET region is eliminated. In addition, the electron-hole concentration is enhanced at the bottom of the trench because an accumulation layer forms. This creates a catenary-type carrier distribution profile (see Fig. 1.91) in the IGBT, which resembles that obtained in a thyristor or pin diode. These improvements lead to a large reduction in the on-state voltage drop until it approaches that of a pin diode, hence approaching the theoretical limit of a silicon device. The latching current density of the UMOS IGBT structure is superior to that of the DMOS structure. This is attributed to the improved hole current flow path in the UMOS structure. As shown in Fig. 1.90c, the hole current flow can take place along a vertical trajectory in the UMOS structure, whereas in the DMOS structure hole current flow occurs below the $n^+$ emitter in the lateral direction. The resistance for the hole current that causes the latch-up is determined only by the depth of the $n^+$ emitter region. A shallow $p^+$ layer can be used, as shown in the figure, to reduce this resistance. As a consequence, the RBSOA of the UMOS IGBT structure is superior to that of the DMOS IGBT structure. Further, because of a very strong percentage of electron current flow in the trench gate IGBT, the turn-off speed of the trench-based IGBT is generally faster than the DMOS-based IGBT. It can be anticipated that trench gate IGBTs will replace the DMOS IGBT structures in the future.
References


1.10 Gate-Commutated Thyristors and Other Hard-Driven GTOs

*Alex Q. Huang*

**Unity Gain Turn-Off Operation**

*Traditional GTO Gate Drive Circuit*

Traditional GTOs are generally designed with a turn-off gain of 3 to 5. This is the result of trade-offs between the performances of the GTO and the current (hence power) requirement its gate drive circuit. *Figure 1.92b* shows the typical turn-off gate drive circuitry for a traditional GTO. A negative turn-off voltage source $V_{OFF}$ is connected to the GTO gate–cathode junction $J_3$ through the turn-off control switch SW. Since both sides of the junction $J_3$ are highly doped, its breakdown voltage $BV_{GC}$ is practically about 20 V and can hardly be increased. The turn-off voltage $V_{OFF}$ is selected below the junction $J_3$ breakdown voltage to avoid constant breakdown of this junction when the GTO is in the off state. To turn off the GTO, switch SW is turned on so the negative turn-off voltage $V_{OFF}$ is applied on the GTO gate–cathode junction. The current originally flowing through the cathode is then diverted to the gate, causing cathode current $I_k$ to decrease and the gate current to increase. Because of the existence of the GTO gate lead stray inductance $L_G$, which is practically on the order of several hundreds of nanohenry determined by the lead structure and length, the cathode current will decrease linearly and the gate current will increase linearly. This current commutation rate is thus given by:

$$\frac{dI_G}{dt} = \frac{V_{OFF}}{L_G}$$  \hspace{1cm} (1.24)

*FIGURE 1.92* Typical turn-off characteristics of a GTO.
The higher the turn-off gate current slew rate, the shorter the storage time. To obtain the shortest storage time, the turn-off voltage is normally selected very close to $BV_{GC}$ to realize highest turn-off gate $dI_C/dt$. The typical turn-off gate $dI_C/dt$ is on the order of several tens of amperes per microsecond, and the typical storage time of a high current GTO is about 20 $\mu$s. Figure 1.93 shows the typical current and voltage waveforms of a GTO turning off with a turn-off gain higher than 1. After the GTO is turned off, its gate current will drop back to 0 slowly by breaking down the GTO gate–cathode junction due to the energy stored in $L_G$. The energy required from the gate driver during this turn-off transition is the integration of the gate current times the turn-off voltage $V_{OFF}$. This energy is significant because the gate current lasts for a long period.

Because of the long transient process, storage time differences among GTO cells become bigger and the non-uniform current redistribution after $t_1$ is significant. The practical RBSOA of a GTO is normally much lower than the 200 kW/cm$^2$ limit set by the dynamic avalanche because of the non-uniform current turn-off (storage time differences and localized dynamic avalanche).

**Unity Turn-Off Gain of the GTO**

If the gate driver of a GTO is very fast so the gate current can increase rapidly to the anode current level and the cathode current decreases to zero before the anode current begins to decay, then the current and voltage waveforms of the device are as shown in Fig. 1.93. According to the definition above, the turn-off gain in this case is unity.

The internal turn-off process of the GTO changes significantly under the unity turn-off gain condition. Most important is that the GTO turn-off is now conducted in the $pnp$ transistor mode after the unity gain is established. Figure 1.94 shows minority carrier distribution during the turn-off transition. Inside the $p$-base, there are two functioning parts of minority carriers (electrons). The first part is the electrons related to the bias of the gate–cathode $pn$-junction; the second part is the electrons related to the forward bias of junction $J_2$. Before the turn-off process at point $t_0$, minority carriers have been accumulated in the $p$-base and $n^-$ region. Starting from $t_0$, the cathode current decreases rapidly and the gate current increases rapidly in the reverse direction. By $t_1$, the cathode current comes to zero so minority carriers associated with the gate–cathode junction are removed. Zero cathode current cuts minority carrier injection from the $n^+$ side into the $p$-base. From this moment, the GTO is like an open-base $pnp$-transistor instead of a $pnpn$ latch-up structure. This difference makes the GTO more rugged during turn-off transition. Negative gate current continues the extraction of minority carriers out from the $p$-base until $t_1$ when they are totally removed.
Advantages of Unity Gain Turn-Off

With unity turn-off gain, the storage time of a GTO is significantly reduced. The storage time in this case is the time required to remove minority carriers in the p-base. In the normal GTO case, the gate current is much less than the anode current so the removal speed is slow. Furthermore, the cathode current is not reduced to zero so minority carrier injection continues during the whole storage phase. With unity turn-off gain, the gate current is as high as the anode current, leading to a rapid carrier removing speed. Also, the cathode current is reduced to zero, hence instantly stopping the minority carrier injection into the p-base. Generally, the storage time of a GTO under unity turn-off gain is about 1 $\mu$s compared with that of about 20 $\mu$s in a normal GTO case with high turn-off gain.

Another important performance improvement with unity gain turn-off is in the RBSOA. As is analyzed above, the GTO current tends to crowd toward the cell with a longer storage time. This process
significantly limits the average instant power a GTO can withstand so a \( \frac{dV}{dt} \) snubber circuitry is normally required to limit the voltage level, hence the instant power stress, during turn-off transition.

GTO cells under unity gain turn-off have a tendency toward uniform current sharing, hence large RBSOA. First, the current filamentation due to the difference of storage time is greatly reduced because the absolute storage time is reduced to less than 1 \( \mu s \). During the voltage rising phase after the storage time, if one cell still shares more current, that cell will have a faster carrier extraction rate and hence will turn off that cell faster. There is therefore a negative feedback process with current sharing instead of a positive one. This negative process is shown in Fig. 1.96.

With this uniform current distribution tendency provided by the unity turn-off gain, a GTO as a whole can be assumed to be more uniform in current sharing and hence can withstand much higher average instant power during turn-off transition. The RBSOA should now be pushed toward a power constant of 200 kW/cm\(^2\) as predicted by Eq. (1.23) (in Section 1.8). This RBSOA is sufficiently large that a GTO should be able to perform turn-off operation even without the help of a \( \frac{dV}{dt} \) snubber. It should also be pointed out again that the onset of dynamic avalanche may not be the actual RBSOA boundary because if it does not initiate a runaway current filament, it is not a destructive one. Experimental results [1] on IGCT turn-off, however, suggest that the dynamic avalanche is not uniform and that it does lead to failure of a device. Unity gain turn-off is therefore effective in removing any current filament problem associated with storage-time differences and the dynamic avalanche soon after the current filament is formed.

### Hard-Driven GTOs

Unity turn-off gain can significantly improve the performance of a GTO in several aspects, including RBSOA and turn-off storage time. Several innovative approaches have been proposed to realize unity turn-off gain. In all approaches, achieving unity turn-off gain is critical. This would require that cathode current be commuted to the gate path very fast. To turn off a 4-kA GTO with unity gain, the commutation rate should be higher than 6 kA/\( \mu s \). This high commutation rate requirement distinguishes the performance of each of the devices discussed below. According to their realizations, they can be classified into two different categories: hard-driven type and MOS-controlled type. Hard-driven type approaches use a powerful gate driver to realize unity turn-off gain. The gate driver supplies the gate current and the gating power. Falling in this category is the integrated gate commutated thyristor (IGCT) [2]. The MOS-controlled approaches use MOSFETs to aid the turn-off process of the GTO. Other than the unity turn-off gain, these approaches also save control power for the turn-off process. Falling in this category are the emitter turn-off (ETO) [3] thyristor and the MOS turn-off (MTO) [4] thyristor.

### IGCT

The key to achieving a hard-driven or unity-gain turn-off condition lies in the gate current commutation rate. A rate as high as 6 kA/\( \mu s \) is required for 4-kA turn-off. Two methods have been demonstrated for the implementation of a hard-driven GTO. The first is to hold the gate loop inductance low enough (3 nH) that a DC gate voltage less than the breakdown voltage of the gate–cathode junction (18 to 22 V) can generate a slew rate of 6 kA/\( \mu s \). This approach is used in the IGCT/GCT [2, 5] (IGCT is an ABB product, GCT is by Mitsubishi, but the concept is the same), where a special low-inductance GTO housing and a
carefully designed gate driver meet this requirement. The power consumption by the GCT driver is greatly reduced compared with that of a conventional GTO driver, since the gate current is present for a much shorter period of time [6]. Figure 1.97 shows the external view of the two commercially available GCTs.

The key disadvantage of the GCT approach is the high cost associated with the low-inductance housing design for the GTO and the low inductance and high current design for the gate driver.

**MTO**

Figure 1.98a shows the turn-off principle of a MTO™ [4, 7] developed by Silicon Power Corporation. The MTO device packages a number of low-voltage MOSFETs within a normal GTO device housing to form a current path that is in parallel with the emitter junction of the GTO. Therefore, the MTO looks...
just like a conventional GTO from the outside. The turn-off is initiated by turning on the MOSFET that shorts the GTO emitter junction. MTO, like the ETO, is therefore a MOS turn-off device requiring very little turn-off gate power. To achieve a high gate current commutation rate, very low gate inductance (<0.1 nH) is required.

Because of the use of the hybrid approach, a prototype 500-A, 4500-V device is available from SPCO. The major problem for the MTO, however, is still the limitation of the RBSOA [7]. This is because the gate current commutation rate is determined by the packaged gate inductance, which has to be reduced to below 0.1 nH. There are three reasons for this. First, in the MTO the commutation rate is determined by

\[
\left( \frac{dI_g}{dt} \right)_{\text{max}} \leq \frac{0.7}{L_g}
\]  

Second, the resistive voltage in the GTO p-base region and the MOSFET determines the peak gate current that can be commutated:

\[
I_{g_{\text{max}}} \leq \frac{0.7}{R_{\text{MOS}} + R_{\text{p-base}}}
\]
Third, since there is no reverse bias voltage applied to the GTO emitter junction in the MTO, it is very easy to become latched again. Snubberless turn-off capability of the MTO is therefore lower than the GCT and ETO.

ETO

The method to achieve unity gain in the ETO thyristor is to insert an additional switch in series with the cathode of the GTO. The cathode of the GTO is the emitter of the internal $npn$ transistor, so the series switch is referred to as the emitter switch and the new device is termed ETO. Turning off the emitter switch generates a high transient voltage long enough to commutate the emitter current to the gate path even with a higher parasitic inductance present. Because of this higher tolerance for parasitic inductance, conventional GTOs can be used in the ETO. An additional switch is connected to the gate of the GTO, and is complementary to the emitter switch. These switches are implemented with many paralleled low-voltage, high-current MOSFETs to minimize the additional conduction loss due to the emitter switch. The typical value for the conduction loss due to the series switch is 0.2 V at the average GTO current rating. The turn-off driving power for the ETO is negligible, since the turn-off is purely due to the removal of a MOSFET gate signal. The ETO in many aspects is similar to the IGBT. For example, the turn-off mechanism used in IGBT is also an emitter turn-off, and the IGBT always turns off in the rugged $pnp$ transistor mode.

Figure 1.99 shows the equivalent circuit and hardware photograph of the developed 4-kA, 6-kV ETO by Virginia Tech. Other lower current rating ETOs have also been demonstrated by Virginia Tech. Because of the use of hybrid approach based on conventional GTO, ETO devices have clear advantages in terms of cost and gate drive power requirement over GCTs. ETO devices also have two other advantages when compared with the GCT. One is its feasibility of having a FBSOA [3, 8], and the other is its simplicity in overcurrent protection [8].

Conclusions

These newly developed GTOs (IGCT, MTO, and ETO) all utilize the unity gain turn-off concept and have dramatically improved performance compared with conventional GTOs. Quantitative comparisons of these devices are provided in a separate section on high-power IGBTs (Section 1.9).
References


1.11 Comparison Testing of Switches

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Pulse Tester Used for Characterization

In a typical power device dynamic test, the device under test (DUT) is initially off, and the high-voltage capacitor bank is charged to set the voltage the DUT will experience during switching. A typical pulse tester is shown in Fig. 1.100 and a typical waveform of the test is shown in Fig. 1.101. The so-called double pulse testing will capture one device turn-on event and one device turn-off event. The double-pulse test consists of the following complete events:

$t_0-t_1$: At time $t_0$, the control system initiates a pulse to the gate driver for the DUT. The DUT turns on and the high voltage capacitor bank charges the load inductor. After the current reaches the desired value at $t_1$, the DUT gate driver is commanded to turn off.

$t_1-t_2$: From time $t_1$ to $t_2$, no changes to the device are seen. During this time, referred to as the storage time, internal processes in the device initiate the turn-off process.

FIGURE 1.100 Pulse tester schematic diagram.
$t_2$–$t_3$: At time $t_2$, the anode voltage begins to rise, as the turn-off process has begun. The freewheeling diode is still reverse-biased so the current cannot yet begin to fall.

$t_3$–$t_4$: At time $t_3$, the anode voltage reaches the bus voltage and the main device current begins to fall. The current that had been flowing through the DUT is commutated into the freewheeling diode. This is the highest stress interval of the turn-off transition, as the current and voltage are simultaneously high during this interval.

$t_4$–$t_5$: At time $t_4$, the main current fall is completed and the current tail phase begins. The current tail continues until $t_5$. At this point the device can be said to have completed the turn-off process.

$t_5$–$t_6$: During this time, the $dI/dt$ snubber resistor carries the current, inducing additional voltage stress on the main DUT. The snubber inductor is charging during this time, and becomes charged at $t_6$. The snubber diode then goes through a reverse-recovery process.

$t_6$–$t_7$: During this time, the DUT is off and blocking a voltage equal to the input capacitor voltage. The current is still freewheeling through the load inductor and the freewheeling diode. This current will continue to circulate for a long time because the only energy dissipation is due to the conduction voltage of the freewheeling diode.

$t_7$–$t_2$: At this time, the controller initiates the second pulse to test the turn-on of the device. Nothing external occurs until $t_9$, which is the end of the turn-on delay time.

$t_9$–$t_{10}$: During this time, the load current begins to commutate into the DUT from the freewheeling diode. The $dI/dt$ snubber inductor determines the rate of current transfer.

$t_{10}$–$t_{11}$: At time $t_{10}$, the load inductor current is completely commutated into the DUT and out of the freewheeling diode. The freewheeling diode undergoes reverse recovery during this period and releases a significant amount of reverse current into the DUT. It is important that the DUT have fully switched on by now or the diode recovery current will induce large power loss.

FIGURE 1.101 Double-pulse tester waveforms.
During this time, the device is on and the current is rising because of the input voltage divided by the load inductance. This is equivalent to the interval $t_0-t_1$ from the first pulse. The same sequence will continue for the turn-off of the second pulse as that for the first pulse.

The current through the device under test is measured with a precision current shunt in series with the cathode (or emitter for an IGBT). All delay times are defined with respect to the actual gate of the device, so gate driver internal delays are not included. Conventionally, fall time is defined as when the current decreases from 90% of its initial value to 10%, but a different definition is used here. For the high-voltage devices, the current tail value can be greater than 10% of the initial current value, so it is unreasonable to include this time in the fall time. Therefore, the definition used here is that the fall time ends and the tail time begins when the current slope visibly changes. This is physically justified because for all three devices the current tail means that the main turn-off process is complete and the open-base $pnp$ transistor is removing the remaining carriers. A sample waveform is shown in Fig. 1.102. Current tail time is defined from the end of the current fall time until the anode/collector current decreases to 1% of the initial current.

**Devices Used for Comparison**

To compare these various semiconductor technologies, two IGBTs, an IGCT, a GCT, and three ETOs were used [1]. One IGBT and the GCT are made by Mitsubishi, and the ETOs have been developed by researchers at Virginia Tech. The other IGBT is made by EUPEC, and the IGCT is from ABB. The IGBTs, CM1200HA-66H and FZ1200R33KF2, are rated for 1200 A (DC) and 3300 V, and are packaged in plastic modules 14 by 19 cm in size. The IGCT and the GCT are both 4500-V devices, which are rated for 4000 A maximum controllable current. The first ETO used, ETO4060s, is rated for 6000 V and 4000 A controllable current, and is based on a Toshiba GTO. The IGCT, the GCT, and the ETO4060s are packaged in 93-mm press-packs and, with gate drivers, have a maximum width of around 20 cm. The second ETO used, ETO1045s, is a small (53-mm) device rated for 4500 V and 1000 A. This ETO is based on a Westcode GTO. The ETO1045s is obviously of a lower rating than the GCT and IGCT, but it uses a fast conventional GTO, whereas the ETO4060s is based on a GTO designed for about 300 Hz. One final device used is a newly designed ETO, the ETO4045A, which is based on an ABB GTO similar to the thyristor used in the IGCT. The average current ratings for the IGCT, GCT, ETO4045A, and ETO4060s are 1200 A, whereas the ETO1045 is suitable for about 450 A average. When the switching losses of the IGBT and a safe

![Fig. 1.102 Switching time definition waveform.](image-url)
temperature margin are considered, the average operating current for this device should be between 600 and 800 A. Figure 1.103 shows most of the devices tested.

One significant difficulty in comparing this type of device is that the ratings, and even the ratings system, are different for the different devices. For GTO-based devices, the current ratings are the peak controllable current, whereas IGBTs use a DC current rating. The IGBTs tested have a controllable current rating of twice the DC rating, which translates to a 2400 A rating in the GTO system. These IGBTs consist of many small dies in parallel, giving a net current density much smaller than that of the GTO-based devices. The rms current for the IGCT, the GCT, and the ETO4045A is about 1800 A, and the RMS current rating of the ETO 4060 is about 1600 A, although the devices have the same average rating (1200 A) from the manufacturers.

**Unity Gain Verification**

Because of the strict requirements on the gate loop stray inductance for the IGCT and the ETO, it is very difficult to insert a current probe directly to monitor the gate current. Fortunately, the unity gain of the IGCT and the ETO can be verified by observing easily probed voltage signals. It is critical for the performance of these devices that unity gain has been achieved, so some effort is made to verify unity gain and predict the maximum current that can be turned off while maintaining the hard-driven condition.

In the case of the IGCT, monitoring the gate-to-cathode voltage at the terminals of the IGCT thyristor can show the unity gain. When the gate voltage becomes \(-20\) V, which is equal to the power supply in
the gate driver, then clearly no voltage drop is occurring across the parasitic gate inductance. This in turn implies that $dl/dt$ is zero, so the gate current has completed commutation. A typical GCT waveform showing the gate voltage is shown in Fig. 1.104. The inside of the GCT driver box is shown in Fig. 1.105.

Unity gain of the ETO can be verified by observing the drain-to-source voltage of the series switch. When the current is commutating, the voltage across this switch quickly rises to the breakdown voltage of the MOSFETs (60 V). When the voltage across this switch begins to fall, then the net cathode current of the GTO is negative, which discharges the output capacitors of the MOSFETs. Therefore, the ETO unity gain corresponds to the falling edge of the emitter switch voltage. A turn-off waveform showing the ETO emitter switch voltage is shown in Fig. 1.106.

Based on the unity gain observation, the rate of current commutation for the devices can be estimated by dividing the anode current by the time required for unity gain. This method yields a lower result than truly occurs because the total current commutated is slightly greater than the anode current due to a reverse recovery effect of the gate to cathode $pn$-junction. Even with this conservative estimation
of the \( \frac{dI}{dt} \) of the gate current, the GCT and the ETO are both capable of approximately 6000 A/\( \mu \)s commutation rate.

**Gate Drive Circuits**

The performance of all semiconductor switches depends on the gate driver circuit. This is especially true for the GCT, where the device will be unable to operate in the snubberless mode if the gate driver is not drawing the gate current out fast enough to achieve unity gain. The drivers for the ETO and IGBT are less difficult to implement since the driver is not required to provide high current.

From a schematic point of view, the GCT driver is very simple, consisting primarily of a capacitor bank and a switch made from many parallel MOSFETs. The PCB layout and component selection is critical because of the very strict stray inductance requirement imposed on the switching loop. Additionally, there is a portion of the driver devoted to turning on the GCT. This is done by injecting a high-current (200-A) pulse into the gate for 5 \( \mu \)s and then injecting 10 A into the gate throughout the on time. This part of the driver dissipates significant power because of the linear transistors controlling the exact current level, but the implementation of this part of the gate driver is simple. The GCT driver contains minimum on-time and off-time protection to allow the device to be always in a uniform state prior to switching. No overcurrent protection is used for the GCT at the driver level. Although the total gating power is still very small compared with the main power, all the gating power must be supplied by an external isolated supply that must have an isolation capability and \( \frac{dV}{dt} \) rejection to match that of the GCT.

Because of the different thyristor design used by ABB in the IGCT, the driving power for this device has been greatly reduced. This is accomplished by increasing the current gain of the thyristor so less gate current is required to maintain the on state. This leads to a DC injection current of only 2 A. In addition, the IGCT driver uses a switching rather than linear circuit for pulse injection, which reduces losses as well.

For the ETO driver, three gates have to be controlled—the GTO current injection, the emitter switch, and the gate switch. Fortunately, the emitter switch and gate switch are easily controlled by using one inverting driver and one non-inverting driver controlled by the same input. The only function of the GTO gate is to inject the turn-on current just as in the case of the GCT. The ETO driver developed at the Center for Power Electronic Systems (CPES) also contains minimum on-time and off-time protection. In addition, the emitter switch MOSFET can be used as a linear resistor to approximate the anode current, which can be used for on-driver overcurrent protection. Like the GCT driver, the ETO driver requires an external isolated power supply, although the power consumption is much lower.
The IGBT driver is very easy to implement, since it has only a single MOS-gate to control. The peak gate current for the tested IGBT is about 10 A, which flows for about 2 $\mu$s at every switching event. The IGBT driver can be used to control actively the $dI/dt$ and $dV/dt$ of the collector, but this feature was not implemented for this test. Information about active driver techniques can be found in many papers such as Lee et al. [2]. The IGBT driver implements an overcurrent protection by means of desaturation detection. IGBT drivers consume so little power that commercial DC-DC converter modules can be used to provide the isolation internally for the high-side switch.

**Forward Conduction Loss Characterization**

The forward current vs. voltage characteristics for all of these devices can be found easily. As can be seen from Fig. 1.107, the thyristors have a clear advantage in conduction loss over the IGBT, even though their active die area is less than that of the IGBT. If the relationship between breakdown voltage and conduction loss is found, the advantage of the latching devices becomes even greater. The 4.5-kV thyristors have the lowest conduction loss, followed by the 6-kV thyristor, and then the IGBT are the worst even if the loss is not normalized to die area. The ABB transparent anode and punch-through base design show an advantage in the forward conduction test, as the higher gain allows the device to latch into an extremely low loss conduction mode. This holds true for the ABB IGCT as well as for the ETO4045A, which is based on an ABB GTO with the same transparent anode and punch-through base design.

**Switching Tests**

Switching performance of high-power devices has been greatly enhanced by the hard-driven GTOs and the HVIGBTs appearing to challenge the slow GTO technology. Typical operation frequencies of the high-power GTOs range from line frequency (50/60 Hz) to a high of about 500 Hz. In contrast, the HVIGBT can be operated at up to 1500 Hz, and the hard-driven GTOs can operate at 1 kHz or more. This increase in frequency leads to dramatically reduced filters and lower distortion in the typical inverter applications.

To evaluate the performance of these devices, they were operated with DC voltages of 1.5 and 2 kV on the pulse tester without any turn-off snubbers. The limiting factor in the amount of current that could be switched off safely was the clamping diode used to limit the voltage spike on the switch. During reverse recovery, the voltage across this diode approaches its breakdown (4.5 kV) at the same time the anode (or collector for IGBTs) voltage of the device under test approaches zero, as circled in Fig. 1.108. For the GCT and the ETOs, no reverse voltage was acceptable because of the lack of either reverse

![Figure 1.107 Forward conduction voltage.](image)
conduction capability (such as an antiparallel diode) or reverse voltage blocking capability. GTO-based devices can achieve reverse voltage blocking easily, but these tested GTOs are anode-shorted types, which trade away the reverse blocking capability for better switching performance, especially in the current tail phase. The ABB design uses a transparent anode rather than anode shorts, which also eliminates the reverse blocking capability. The transparent anode technology makes the current gain of the device change as a function of the current flowing so that it will have a high gain at low current and a lower gain at high current. The switching losses for each device were calculated by first multiplying the voltage across the device by the current being conducted, and then integrating this instantaneous power during the switching time to find the switching loss. The results of the switching loss tests were compared for the IGBT, the GCT, and the ETOs. These results are shown for a 2-kV bus in Fig. 1.109.

As expected, the IGBT holds the advantage in this test with the lowest turn-off loss overall. Surprisingly, the loss of the GCT and the ETO1045 is only marginally higher than the IGBT loss. The primary advantage of the IGBT in switching loss is in the initial voltage rising phase, which occurs much faster than in the thyristors. This is because the MOSFET channel in the IGBT can turn off faster than the \textit{npn} transistor.

**FIGURE 1.108** Typical turn-off waveform.

**FIGURE 1.109** A 2-kV snubberless switching loss.
in the GTOs, and the channel is better distributed through the IGBT than are the gates of the GTOs. The amount of carrier stored in the GTOs is also higher than in the IGBT, resulting in slower $dV/dt$. It is not surprising that the ultrahigh-voltage ETO4060 has significantly more switching loss than the lower-voltage devices. The probable reasons for the high switching loss of this device are a high carrier lifetime in the GTO, a strong \textit{pnp} transistor, which can maintain the current longer with the base open, and a GTO design optimized for low-frequency, high-power operation. The theory of hard-driven GTOs predicts no improvement in turn-off loss when compared with traditionally driven GTOs, only an improved safe operating area and higher speed. This shows that the GCT is very well optimized for performance as well as for a low internal inductance. The transparent anode of the ABB IGCT proved a disadvantage in this test, as switching times and switching losses were noticeably worse than with the anode-shorted devices.

As can be seen in \textbf{Fig. 1.110}, the switching times for all of these devices are short and very consistent. The ETOs and the GCT have long storage times at very low current levels, but the storage time is very consistent at 600 A and beyond. The current fall times for all devices characterized except the IGCT are around 250 ns and are essentially independent of the current being switched, as shown in \textbf{Fig. 1.111}. The IGCT has a very long current fall time at low current levels, although the speed improves at higher currents. The IGCT tail has a very large magnitude, which again shows that the anode-shorted structure of the GCT and the ETOs offers advantages in this area.

\textbf{FIGURE 1.110} Storage (or delay) time comparison.

\textbf{FIGURE 1.111} Fall time comparison.
Because of the large (10 $\mu$H) turn-on inductor, the turn-on loss for all devices is negligible. All the thyristors hold a very slight advantage over the IGBT in terms of voltage fall time at turn-on, but the current is so low during this time that there is no significant difference in loss. It must be noted that the IGBT can be operated without the turn-on snubber at the expense of significantly increased switching loss, but doing so requires a more complex gate driver design. This is due to the ability of the IGBT to control the exact collector current by operating in the linear region. The GCT completely lacks this operating mode. Theoretical analysis predicts the existence of this forward-biased Safe Operating Area for the ETO [3], but no experimental verification has been performed except at low current [4]. For current tail comparison, the tail current was examined on a very high resolution (10 A/div) to see all the effects. Immediately after the main current fall, the tail current decreases rapidly for all the devices tested. However, the current tail can take a long time to finish decreasing to zero after this initial fast fall. The detail of the GCT current tail is shown in Fig. 1.112 after turning off 1200 A. The current tail can indicate the strength of the $pnp$ transistor within an IGBT or a GTO. The long tail observed for the ETO4060 indicates a stronger $pnp$, which helps reduce the conduction losses. The GCT demonstrates the shortest current tail of all of the devices tested, which is further evidence of the very good internal design. The drawback of this performance is that the effective current gain of the GCT is reduced, thus requiring more DC gate current injection during conduction. The IGBT and the ETO1045 have only slightly worse current tails than the GCT.

Traditionally, the GTO switching frequencies were limited by the times required for the GTO to complete the switching transitions. In particular, a very long minimum off-time had to be observed due to some parts of the GTO remaining latched for more than 100 $\mu$s. The devices tested here all have very fast switching times, but the switching loss is rather high because of the very large currents and voltages considered. Therefore, the switching frequency is thermally limited by the switching loss. Soft switching techniques may allow these devices to achieve much higher operating frequencies (~10 kHz) if the switching loss can be reduced.

**Discussion**

Packaging technology is very different for the IGBT modules compared with GTO packaging. The IGBT modules use many parallel dies, which are wire-bonded and housed in a plastic module. Since a GTO can be fabricated on a single wafer, press-pack ("hockey-puck") housings are utilized. The reliability record for the press-pack devices is much higher than wire-bond modules, largely due to a better tolerance
for thermal cycling. Additionally, the press-pack allows double-sided cooling to lower the thermal impedance. However, the IGBT achieves similar thermal impedance overall because of the much larger die area and the consequently large baseplate. The IGBT baseplate is electrically isolated from the heat sink, but the press-pack heat sinks are directly connected to the anode and cathode terminals. As a result, liquid-cooled systems with press-pack devices must rely on oil or deionized water to prevent the coolant from conducting current. The main advantage of the IGBT module is its ease of use, with the isolated baseplate leading to easy heat-sinking. The collector and emitter terminals are conveniently located for connection to a laminated busbar to reduce the parasitic inductance and hence the voltage spike. Additionally, the IGBT module does not require any external mechanical clamp for mounting, as the press-pack housing requires. The reliability of the press-pack is a key issue, and this package is preferred for many applications where long life is necessary.

Although failures are obviously unwanted, the characteristics of the device after a failure should be considered. This can make a big difference in how much damage is done to the rest of a system and how difficult repair will be. After a failure, any of these devices will become short-circuited. The current will then increase until either all the energy available has been consumed or an external circuit acts to stop the fault current. For the wire-bond IGBT, all the current will concentrate into the die that broke down. This will usually destroy the wire bonds for that die as a result of the huge current flowing. After failure, the IGBT can become an open circuit. This is a very dangerous condition for series-connected devices or multilevel converters, as the voltage will no longer be shared, thus exposing the other devices in the chain to the risk of overvoltage [5]. The press-pack devices will remain shorted since the die is directly connected with the metal contacts. There is some concern about the wire-bond MOSFETs in the ETO emitter and gate switches, although no failure of these MOSFETs has yet been seen even after destruction of the GTO. Another issue related to the packaging is explosion damage. The press-pack is very strong, and as a result explosions are very unlikely in this type of package. Plastic modules can easily shatter the housing, which leads to damage to nearby components.

As previously mentioned, an IGBT can actively control the collector voltage and current during the switching events. This feature of the device can lead to reduced EMI as well as elimination of the $\frac{dI}{dt}$ (turn-on) snubber. However, elimination of this snubber in high-power, quasi-zero impedance source (voltage-fed) converters may not be desirable because of the other benefits the snubber offers. These include elimination of damage due to cross-conduction of bridge switches (“shoot-through”), or load short-circuiting, and improved fault management. If the rate of rise of current in a fault condition is controlled, a fast device such as the (I)GCT, ETO, or IGBT can respond in time to turn off the fault current with the semiconductor switches. For GTO systems, the GTO could not respond in time to interrupt a fault current, so the protection commonly used was to turn all the bridge switches on and wait for fuses to open. The ability of the ETO and IGBT to automatically detect and respond to overcurrents enhances the safe operation of high-power systems. In addition, the IGBT can self-limit the current that will be conducted, so operation within the switching capability of the device’s can be ensured. Thyristor devices will conduct an extremely high surge current that is much higher than their interrupting capability, which requires control logic to prevent the devices from switching off during this time.

**Comparison Conclusions**

As can be seen from the switching times, all of the devices tested here offer very fast switching times relative to their power ratings. In addition, even the worst conduction loss from the IGBT is still acceptable when compared with the blocking voltage. For very high power systems, the IGCT, the GCT, the ETO4045A, and the ETO4060s are capable of handling extremely high power levels. The GCT is very fast for its high rating, and the only drawback is the difficult to construct gate driver and its power consumption. The ABB IGCT and the ETO4045A trade away switching loss to reduce driver power and conduction loss, so these devices are particularly suited to advanced topologies that reduce the necessary switching frequency or to soft-switching applications that can reduce the switching loss. The ETO4060 offers very high ratings with minimal driving power, even though the switching is not quite as good as
the GCT; however, it is better than the IGCT. The IGBT offers the best switching speed and loss of any of the devices tested and the simplest drive. However, the GCT and small ETO are amazingly close to the IGBT in switching loss considering their latching nature and nearly 50% higher voltage rating. The performance of all devices tested here is very good, especially compared with the conventional GTO applications.

References

1. K. Motto, Y. Li, and A.Q. Huang, Comparison of the state-of-the-art in high power IGBTs, IGCTs, and ETOs, in *Conf. Rec. IEEE-APEC*, 2000, 1129–1136.
4. Z. Xu, Y. Bai, Y. Li, and A.Q. Huang, Experimental demonstration of the forward biased safe operation area of the emitter turn-off thyristor, in *Proc. CPES-VT Seminar*, 2000, 448–455.